LCD Controller IC

KS-LTSV-SD (LVDS)

Hardware Manual

April 2011, Second Edition (Japanese version)

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KS-LTSV-SD (LVDS)

(Note)　Silk screen print in the above picture is a composite. The actual print may differ.

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● Introduction ●

First of all, thank you for having purchased our LCD controller IC (KS-LTSV-SD (LVDS)) and the touch panel controller IC (KS-R8TPC) (the "Product"). This hardware manual (the "Manual") provides an overview of the Product. We hope that you will read the Manual carefully and make use of it for efficient development.

● Important Information ●

1. The Product and this Manual may change without notice. Before using the Product, obtain the newest catalog, manual, etc., from the company website.

2. The Product is not designed to be used in systems or devices that can cause death, injury, or serious physical or environmental damage directly due to any malfunction of the Product (life support device, nuclear facility equipment, aircraft, traffic control equipment, various safety devices, etc.). Danger and damage due to the Product being used in the foregoing systems or devices are the sole responsibility of the customer.

3. We assume no responsibility for any damages due to the use or the operation of the Product in a misguided or wrongful way.

4. The usage examples outlined herein are only an explanation of the Product functions. We assume no responsibility for any complaints, accidents, or any disadvantages which may be caused by the use on the basis of the examples outlined in this Manual.

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1. Composition of the LCD Controller IC and the Touch Panel Controller LCD

1) KS-LTSV-SD (LVDS) (LCD controller IC)

   KS-LTSV-SD (LVDS) is broadly applicable to the LVDS LCD, including "LMTM080SVGNLA series" (manufacturer: DENSITRON), "GKTS80SPAH series" (manufacturer: SGD), and color SVGA TFT LCD "NL8060BC31 series" (manufacturer: NEC), etc.

2) KS-R8TPC (Touch panel controller)

   KS-R8TPC is a CPU device with 2 channels, 8-bit A/D conversion (manufacturer: Renesas, model: R5F211B4SP).

   (Manufacturer of the CPU and product number may change without notice.)

   LCD display and touch panel control become possible by using the above set of two. Additionally, display is also possible using only the LCD controller IC.

2. Overview and Features of the Product

KS-LTSV-SD (LVDS) is an LCD controller developed for embedded systems, with the following characteristics.

1) This LCD controller is SVGA TFT color LCD-compatible (Interface is LVDS). The LCD controller is equipped with a built-in LVDS interface. We guarantee that signal distance for the LVDS is 2m.

2) The frame buffer memory is SDR SDRAM-compatible. When using the SDR SDRAM (2M×16-bits×4 banks), you can select a wide area of 2,048 × 1,024 pixels × 4 pages to 800×600 pixels.

3) Color can be displayed in 2 modes: 64 colors in 4,096 color mode (palette format) × 2 pages and 65,536 color mode × 1 page.

4) By making the screen one page per area, 65,536 colors can be displayed. (There are function restrictions such as blinking, etc.).

5) Two-layer superimposed display is possible. (Only the 64 colors in 4,096 color mode).

6) When a flash-ROM is installed to the CPU bus, short videos can be played.

7) The Tiny-accelerator function allows high-speed drawing of lines and fill-ins of rectangular shapes

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8) There is an automatic switch display function per pixel, which decreases the load on the CPU.

9) Design is easy with only knowledge of the Host-CPU. LCD expertise is not necessary.

10) The Host-CPU is most compatible with the H8 Host-CPU (Hitachi) and SH Host-CPU. (Interface with 3.3V Host-CPU is possible.)

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3. System Configuration Diagram

The outline framework for KS-LTSV-SD (LVDS) is as follows. The customer only needs to prepare a SDR SDRAM in order to complete the LCD controller. And, by preparing a large flash memory, the LCD controller reads data automatically, image display is also possible.

HOST CPU

Host CPU Interface
A1-A22,D0-D15,RD#,WRH#,
WRL#,WAIT#, READY#,
BACK#, BREQ#, CS#, etc

3.3V System
Flash — Rom (for storing image data)

16-bit CPU_BUS

KS-LTSV-SD (LVDS)

LVDS pin

CLK+, CLK-, D2+, D2-,
D1+, D1-, D0+, D0-, etc

LCD Module

SVGA LCD

LVDS pin

Touch Panel

3.3V System SDRAM

DQ0-15, A0-A11, DQMH, DQML, WE#,
CAS#,RAS#,CS#,BA0,BA1,
CLK, CKE, etc

16-bit SDRAM_BUS

PWM ON/OFF pin

BackLight Power

3.3V system
Crystal oscillator

Serial pin

CLK pin

Power Input +3.3V,+2.5V,+1.2V

Touch Panel Controller Circuit (KS-R8TPC etc.)
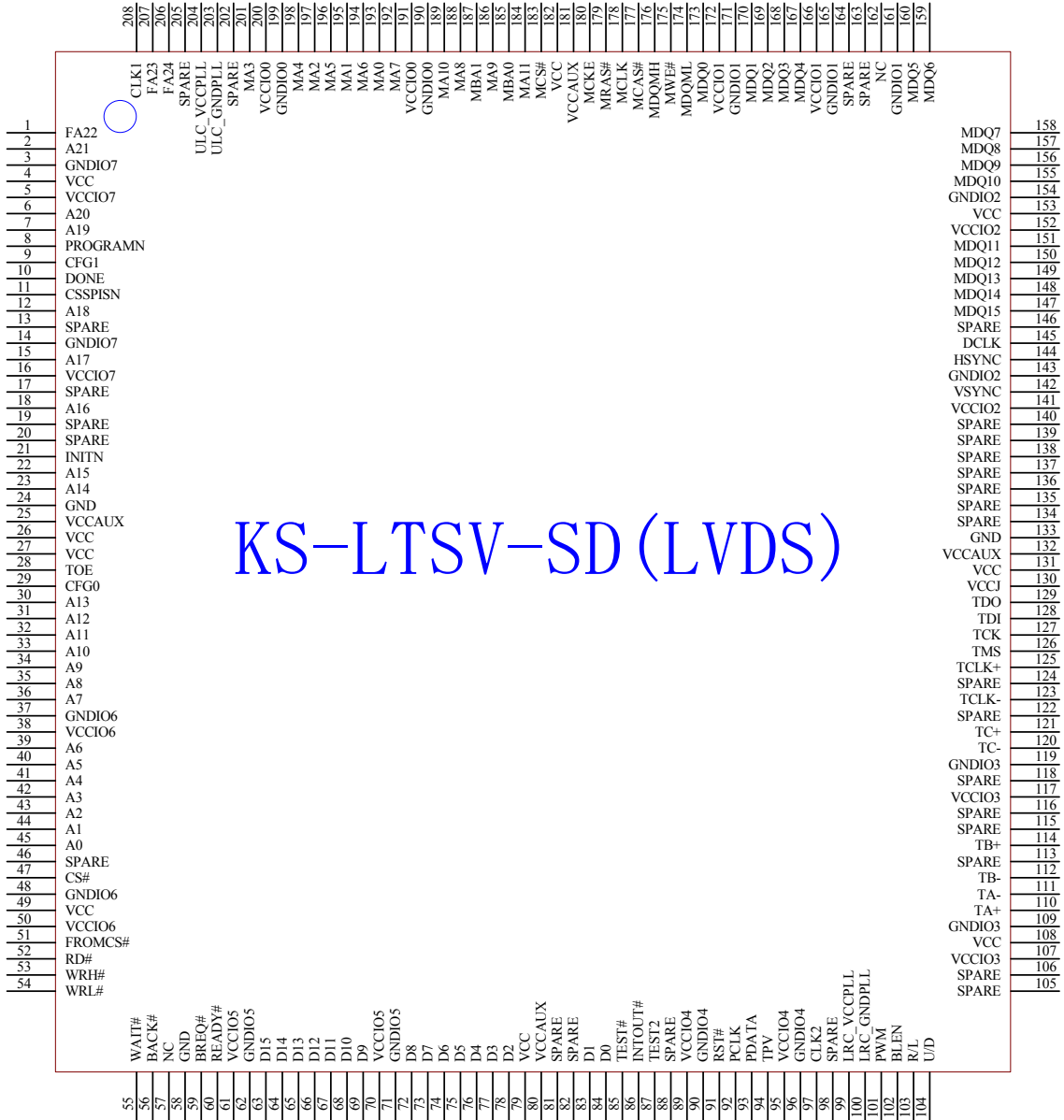
PCLK, TPV, PDATA, etc

Note 1. The blue areas indicate the LCD controller and the touch panel controller.
Note 2. When the touch panel (KS-R8TPC) is not necessary, its circuit part is deletable.

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4. Pins

Diagram) Pinout Diagram

KS-LTSV-SD (LVDS)

Left side pins:

Pin	Signal
1	FA22
2	A21
3	GNDIO7
4	VCC
5	VCCIO7
6	A20
7	A19
8	PROGRAMN
9	CFG1
10	DONE
11	CSSPISN
12	A18
13	SPARE
14	GNDIO7
15	A17
16	VCCIO7
17	SPARE
18	A16
19	SPARE
20	SPARE
21	INITN
22	A15
23	A14
24	GND
25	VCCAUX
26	VCC
27	VCC
28	TOE
29	CFG0
30	A13
31	A12
32	A11
33	A10
34	A9
35	A8
36	A7
37	GNDIO6
38	VCCIO6
39	A6
40	A5
41	A4
42	A3
43	A2
44	A1
45	A0
46	SPARE
47	CS#
48	GNDIO6
49	VCC
50	VCCIO6
51	FROMCS#
52	RD#
53	WRH#
54	WRL#

Bottom side pins:

Pin	Signal
55	WAIT#
56	BACK#
57	NC
58	GND
59	BREQ#
60	READY#
61	VCCIO5
62	GNDIO5
63	D15
64	D14
65	D13
66	D12
67	D11
68	D10
69	D9
70	VCCIO5
71	GNDIO5
72	D8
73	D7
74	D6
75	D5
76	D4
77	D3
78	D2
79	VCC
80	VCCAUX
81	SPARE
82	SPARE
83	D1
84	D0
85	TEST#
86	INTOUT#
87	TEST2
88	SPARE
89	VCCIO4
90	GNDIO4
91	RST#
92	PCLK
93	PDATA
94	TPV
95	VCCIO4
96	GNDIO4
97	CLK2
98	SPARE
99	LRC_VCCPLL
100	LRC_GNDPLL
101	PWM
102	BLEN
103	R/L
104	U/D

Right side pins:

Pin	Signal
105	SPARE
106	SPARE
107	VCCIO3
108	VCC
109	GNDIO3
110	TA+
111	TA-
112	TB-
113	SPARE
114	TB+
115	SPARE
116	SPARE
117	VCCIO3
118	SPARE
119	GNDIO3
120	TC-
121	TC+
122	SPARE
123	TCLK-
124	SPARE
125	TCLK+
126	TMS
127	TCK
128	TDI
129	TDO
130	VCCJ
131	VCC
132	VCCAUX
133	GND
134	SPARE
135	SPARE
136	SPARE
137	SPARE
138	SPARE
139	SPARE
140	SPARE
141	VCCIO2
142	VSYNC
143	GNDIO2
144	HSYNC
145	DCLK
146	SPARE
147	MDQ15
148	MDQ14
149	MDQ13
150	MDQ12
151	MDQ11
152	VCCIO2
153	VCC
154	GNDIO2
155	MDQ10
156	MDQ9
157	MDQ8
158	MDQ7

Top side pins:

Pin	Signal
208	CLK1
207	FA23
206	FA24
205	SPARE
204	ULC_VCCPLL
203	ULC_GNDPLL
202	SPARE
201	SPARE
200	MA3
199	VCCIO0
198	GNDIO0
197	MA4
196	MA2
195	MA5
194	MA1
193	MA6
192	MA0
191	MA7
190	VCCIO0
189	GNDIO0
188	MA10
187	MA8
186	MBA1
185	MA9
184	MBA0
183	MA11
182	MCS#
181	VCC
180	VCCAUX
179	MCKE
178	MRAS#
177	MCLK
176	MCAS#
175	MDQMH
174	MWE#
173	MDQML
172	MDQ0
171	VCCIO1
170	GNDIO1
169	MDQ1
168	MDQ2
167	MDQ3
166	MDQ4
165	VCCIO1
164	GNDIO1
163	SPARE
162	SPARE
161	NC
160	MDQ5
159	MDQ6

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The following table indicates pin assignments (list of pin numbers and signal names) for KS-LTSV-SD (LVDS).

In this Manual, we have provided the reference circuits as examples. (However, operation of these circuits is not guaranteed. Be aware that the circuit may not operate due to certain circumstances and conditions.)

Table 1) KS-LTSV-SD (LVDS)

Pin No	Pin Name	Interface	Pin No	Pin Name	Interface
1	FA22	Address signal for FROM (Output)	105	SPARE	No connection
2	A21(*1)	Generic Host-CPU address bus (I/O)	106	SPARE	No connection
3	GNDIO7	0V	107	VCCIO3	+2.5 V
4	VCC	+1.2V	108	VCC	+1.2V
5	VCCIO7	+3.3V	109	GNDIO3	0V
6	A20(*1)	Generic Host-CPU address bus (I/O)	110	TA+	To LCD panel
7	A19(*1)		111	TA−	
8	PROGRAMN	10k Pull-up	112	TB−	
9	CFG1	10k Pull-up	113	SPARE	No connection
10	DONE	10k Pull-up	114	TB+	To LCD panel
11	CSSPISN	4.7k Pull-up	115	SPARE	No connection
12	A18(*1)	Generic Host-CPU address bus (I/O)	116	SPARE	
13	SPARE	No connection	117	VCCIO3	+2.5V
14	GNDIO7	0V	118	SPARE	No connection
15	A17(*1)	Generic Host-CPU address bus (I/O)	119	GNDIO3	0V
16	VCCIO7	+3.3V	120	TC−	No connection
17	SPARE	No connection	121	TC+	
18	A16(*1)	Generic Host-CPU address bus (I/O)	122	SPARE	No connection
19	SPARE	No connection	123	TCLK−	To LCD panel
20	SPARE		124	SPARE	No connection
21	INITN	10k Pull-up	125	TCLK+	To LCD panel
22	A15(*1)	Generic Host-CPU address bus (I/O)	126	TMS	Signal for configuration 10k Pull-up
23	A14(*1)		127	TCK	Signal for configuration 2.2k Pull-down
24	GND	0V	128	TDI	Signal for configuration
25	VCCAUX	+3.3V	129	TDO	
26	VCC	+1.2V	130	VCCJ	+3.3V
27	VCC		131	VCC	+1.2V
28	TOE	10k Pull-up	132	VCCAUX	+3.3V
29	CFG0	2.2k Pull-down	133	GND	0V
30	A13(*1)	Generic Host-CPU address bus (I/O)	134	SPARE	No connection
31	A12(*1)		135	SPARE	
32	A11(*1)		136	SPARE	
33	A10(*1)		137	SPARE	
34	A9(*1)		138	SPARE	
35	A8(*1)		139	SPARE	
36	A7(*1)		140	SPARE	

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37	GNDIO6	0V	141	VCCIO2	+3.3V
38	VCCIO6	+3.3V	142	VSYNC	Frame signal output
39	A6(*1)	Generic Host-CPU address bus (I/O)	143	GNDIO2	0V
40	A5(*1)		144	HSYNC	No use
41	A4(*1)		145	DCLK	No use
42	A3(*1)		146	SPARE	No connection
43	A2(*1)		147	MDQ15	SDR SDRAM data bus
44	A1(*1)		148	MDQ14	
45	A0(*1)		149	MDQ13	
46	SPARE	No connection	150	MDQ12	
47	CS#	Generic Host-CPU (Input)	151	MDQ11	
48	GNDIO6	0V	152	VCCIO2	+3.3V
49	VCC	+1.2V	153	VCC	+1.2V
50	VCCIO6	+3.3V	154	GNDIO2	0V
51	FROMCS#(*1)	Chip select signal for FROM (Tristate output)	155	MDQ10	SDR SDRAM data bus
52	RD#(*1)	Generic Host-CPU (I/O)	156	MDQ9	
53	WRH#	Generic Host-CPU (Input)	157	MDQ8	
54	WRL#		158	MDQ7	
55	WAIT#	Generic Host-CPU (Tristate output)	159	MDQ6	
56	BACK#	Generic Host-CPU (Input)	160	MDQ5	
57	NC	No connection	161	GNDIO1	0V
58	GND	0V	162	NC	No connection
59	BREQ#	Generic Host-CPU (Output)	163	SPARE	
60	READY#		164	SPARE	
61	VCCIO5	+3.3V	165	GNDIO1	0V
62	GNDIO5	0V	166	VCCIO1	+3.3V
63	D15	Generic Host-CPU data bus (I/O)	167	MDQ4	SDR SDRAM data bus
64	D14		168	MDQ3	
65	D13		169	MDQ2	
66	D12		170	MDQ1	
67	D11		171	GNDIO1	0V
68	D10		172	VCCIO1	+3.3V
69	D9		173	MDQ0	SDR SDRAM data bus
70	VCCIO5	+3.3V	174	MDQML	SDR SDRAM control signal
71	GNDIO5	0V	175	MWE#	
72	D8	Generic Host-CPU data bus (I/O)	176	MDQMH	
73	D7		177	MCAS#	
74	D6		178	MCLK	SDR SDRAM clock
75	D5		179	MRAS#	SDR SDRAM control signal
76	D4		180	MCKE	
77	D3		181	VCCAUX	+3.3V
78	D2		182	VCC	+1.2V
79	VCC	+1.2V	183	MCS#	SDR SDRAM control signal
80	VCCAUX	+3.3V	184	MA11	SDR SDRAM address bus
81	SPARE	No connection	185	MBA0	SDR SDRAM bank address
82	SPARE		186	MA9	SDR SDRAM address bus

83	D1	Generic Host-CPU data bus (I/O)	187	MBA1	SDR SDRAM bank address
84	D0		188	MA8	SDR SDRAM address bus
85	TEST#	+3.3V	189	MA10	
86	INTOUT#	Interrupt request output	190	GNDIO0	0V
87	TEST2	No connection (test signal output)	191	VCCIO0	+3.3V
88	SPARE	No connection	192	MA7	SDR SDRAM address bus
89	VCCIO4	+3.3V	193	MA0	
90	GNDIO4	0V	194	MA6	
91	RST#	Reset circuit	195	MA1	
92	PCLK	To KS-R8TPC	196	MA5	
93	PDATA		197	MA2	
94	TPV		198	MA4	
95	VCCIO4	+3.3V	199	GNDIO0	0V
96	GNDIO4	0V	200	VCCIO0	+3.3V
97	CLK2	Clock etc.	201	MA3	SDR SDRAM address bus
98	SPARE	No connection	202	SPARE	No connection
99	LRC_VCCPLL	+3.3PLL	203	ULC_GNDPLL	0V
100	LRC_GNDPLL	0V	204	ULC_VCCPLL	+3.3 PLL
101	PWM	To backlight part	205	SPARE	No connection
102	BLEN		206	FA24	Address signal for FROM (output)
103	R/L	To LCD panel	207	FA23	
104	U/D		208	CLK1	Clock etc.

Precautions

(*1) These ports are in the following states during image data transfer and when image data transfer is not occurring (normal state).

- During image data transfer

    A21~A0　　　・・・　Output

    FROMCS#　・・・　Output

    RD#　　　・・・　Output

- Image data transfer not occurring (Normal state)

    A21~A0　　　・・・　Input

    FROMCS#　・・・　Hi impedance

    RD#　　　・・・　Input

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【Reference Circuits】

(1) Reference Circuit Diagram of the LCD Controller IC Area
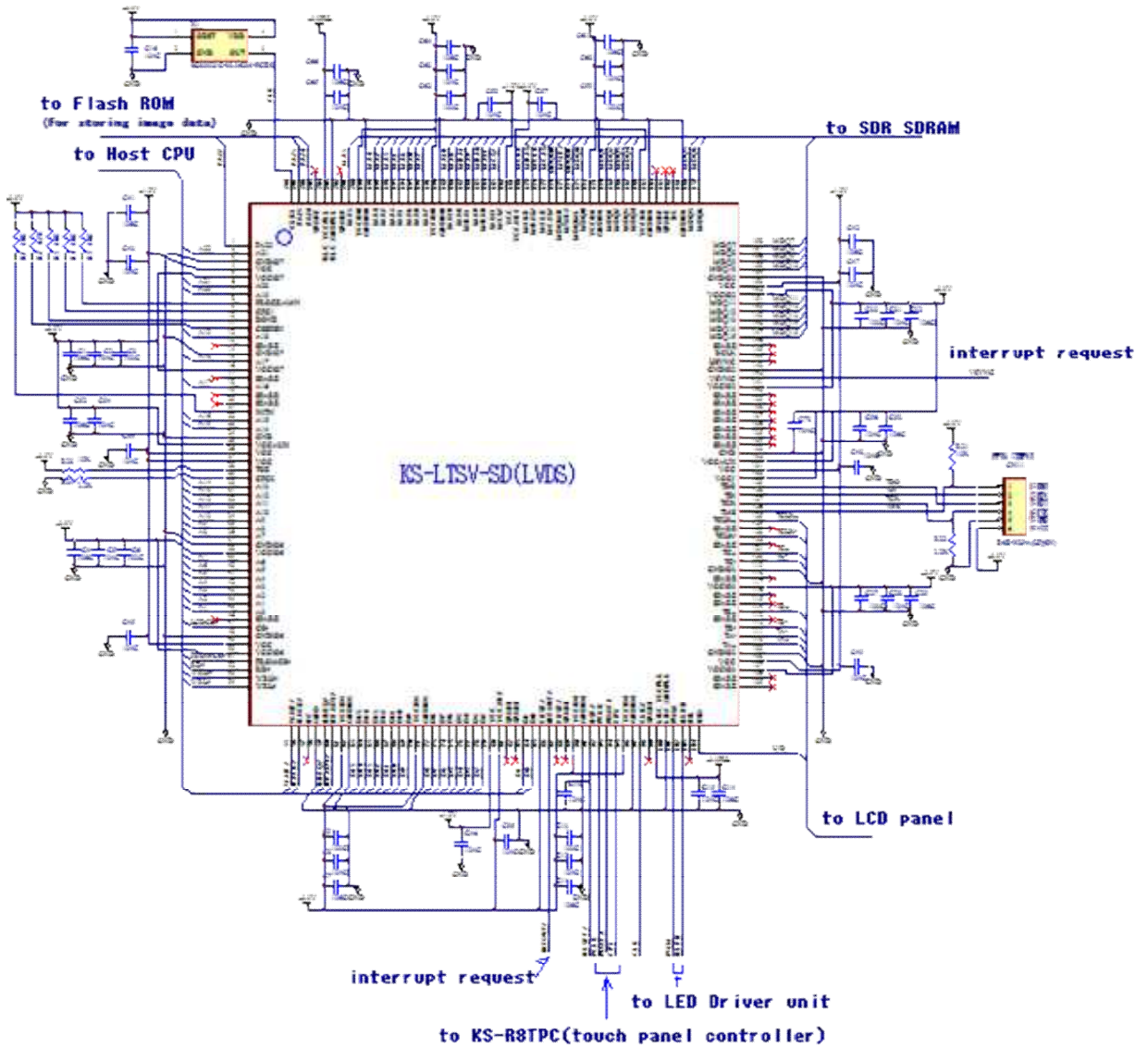
(Connection and Precautions)

・ Quartz Module

Although the quartz module contains the SG8002 (EPSON); any product with a frequency of 38.362MHz can be used.

There are two clock pins (No.97 pin and No.208 pin) for the LCD controller. Provide each clock from same quartz module.

・ About the CPU Bus

Connect to Hitachi-manufactured H8 Host-CPU, SH-2 Host-CPU, or SH-3, 4 processor, etc.

For the address bus, connect the A22~A1 from the CPU to the A21~A0 pins of the LCD controller.

When using the H8 Host-CPU, SH-2 Host-CPU, or SH-3 processor, connect the WAIT# signal from the LCD controller to the WAIT# pin input of the CPU. Always pull up with a resistance of 4.7k~10k for the WAIT# signal. When using the SH-4 processor, connect the READY# signal from the LCD controller to the RDY# pin input of the CPU.

When installing the FROM for images and using the image data transfer function of the LCD controller, the LCD controller accesses the FROM for images, so it is necessary to release the CPU bus. In that case, connect the BREQ# signal and BACK# signal of the LCD controller to the BREQ# pin and BACK# pin of the CPU.

When transferring image data, I/O direction is switched for some signals of the CPU bus. Regarding the switch timing of the I/O direction, refer to "5. Electrical Characteristics (DC, AC), Access Timing Specifications".

・ Reset Signal

The LCD controller provides RESET# input pins for the LCD controller. The internal circuit is reset by ACTIVE LOW. Connect the reset signal used by the CPU, etc. Additionally, if there is noise on the reset signal line, mount a capacitor with the capacity of about 104 near the RESET# input pin, in order to prevent inadvertent resets.

・ Connection to the SDR SDRAM

Refer to "(2) Reference Circuit of the SDR SDRAM" below.

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・ Connection to the FROM for image

Refer to "(3) Reference Circuit of the FROM for images" below.

・ Connection to the LCD

Refer to "(4) Reference Circuit of the LCD I/F" below.

・ Connection to the Touch Panel Controller (KS-R8TPC)

KS-R8TPC can be connected directly. For more details, refer to "Touch panel controller IC KS-R8TPC hardware manual".

When using the LCD controller only, use the control signals (PCLK, PDATA, TPV) with the open state.

・ Arrangement of the Bypass Capacitor

Be particularly careful about the arrangement of the bypass capacitor. When a four- layer board is impossible, bring as close to the LSI VCC pin as possible.

・ Power Supply for PLL

PLL is used inside the LCD controller. As the LRC_VCCPLL and ULC_VCCPLL power supply pins for the PLL are susceptible to noise, make a single point connection (connect via a 0Ω resistor) with other power supplies as shown in the diagram below.

Moreover, in order to further eliminate the effect of noise, it is recommended to insulate from other power supplies using an inductor. (Replace 0Ω resistor with inductor.)

Inductor Specifications (Example)

■ Package size   0805 package (2×1.25)
■ Rated current   1A
■ Inductance   0.1µH and over

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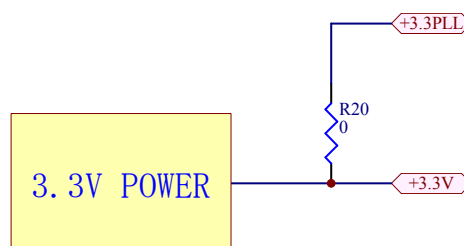
(2) Reference Circuit of the SDR SDRAM (IS42S16800E-7TL)

to LCD Controller
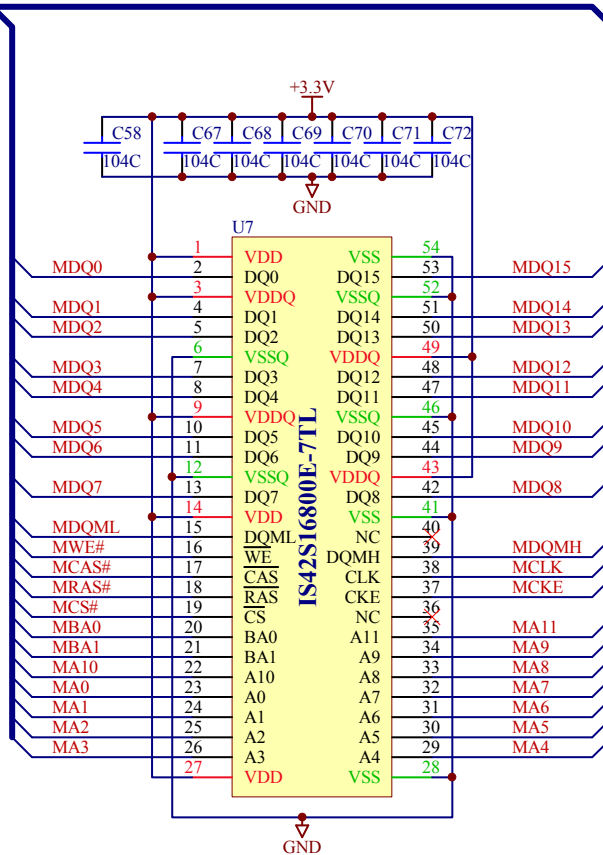
Be careful with the connection of the bypass capacitor; place near the VCC. Additionally, for the pattern length, make sure the distance from the LCD controller is under 10cm. It is recommended that the wiring use the fewest number of vias as possible, and that isometric wiring is used.

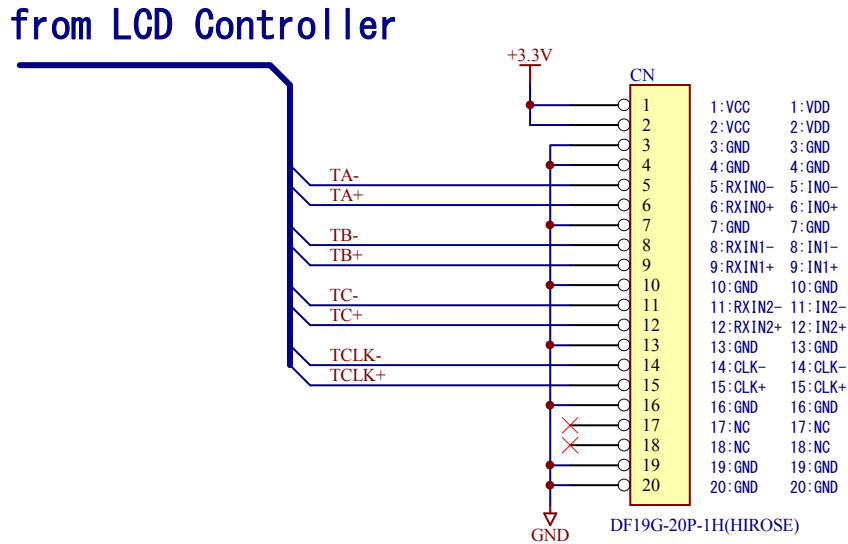Use the SDR SDRAM with 7nS and under (IS42S16800E-7TL (ISSI), IS42S16800E-6TLI, etc.).

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(3) Reference Circuit of FROM for images (S29GL512P10TFI)

to Host CPU   from LCD Controller

+3.3V
C74 104C
GND

U2
S29GL512P10TFI

Pin	Name		Name	Pin	Net
FA23	1	A23	A24	56	FA24
FA22	2	A22	NC	55	
A16	3	A15	A16	54	A17
A15	4	A14	BYTE#	53	
A14	5	A13	VSS	52	
A13	6	A12	DQ15/A-1	51	D15
A12	7	A11	DQ7	50	D7
A11	8	A10	DQ14	49	D14
A10	9	A9	DQ6	48	D6
A9	10	A8	DQ13	47	D13
A20	11	A19	DQ5	46	D5
A21	12	A20	DQ12	45	D12
WRH#	13	WE#	DQ4	44	D4
RESET#	14	RESET#	VCC	43	
A22	15	A21	DQ11	42	D11
	16	WP#/ACC	DQ3	41	D3
	17	RDY/BY#	DQ10	40	D10
A19	18	A18	DQ2	39	D2
A18	19	A17	DQ9	38	D9
A8	20	A7	DQ1	37	D1
A7	21	A6	DQ8	36	D8
A6	22	A5	DQ0	35	D0
A5	23	A4	OE#	34	RD#
A4	24	A3	VSS	33	
A3	25	A2	CE#	32	FROMCS#
A2	26	A1	A0	31	A1
	27	RFU	RFU	30	
	28	RFU	VIO	29	

+3.3V
R7
10K

GND

The above diagram is the connection example to the flash memory "S29GL512P10TFI" (SPANSION).

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(4) Reference Circuit of the LCD I/F

・ Connection example to SVGA-TFT LCD (DENSITRON・SGD)

from LCD Controller


```
                                    +3.3V        CN
                                                 1      1:VCC     1:VDD
                                                 2      2:VCC     2:VDD
                                                 3      3:GND     3:GND
                                                 4      4:GND     4:GND
         TA-                                     5      5:RXIN0-   5:IN0-
         TA+                                     6      6:RXIN0+   6:IN0+
                                                 7      7:GND      7:GND
         TB-                                     8      8:RXIN1-   8:IN1-
         TB+                                     9      9:RXIN1+   9:IN1+
                                                 10     10:GND     10:GND
         TC-                                     11     11:RXIN2-  11:IN2-
         TC+                                     12     12:RXIN2+  12:IN2+
                                                 13     13:GND     13:GND
         TCLK-                                   14     14:CLK-    14:CLK-
         TCLK+                                   15     15:CLK+    15:CLK+
                                                 16     16:GND     16:GND
                                                 17     17:NC      17:NC
                                                 18     18:NC      18:NC
                                                 19     19:GND     19:GND
                                                 20     20:GND     20:GND
                              GND        DF19G-20P-1H(HIROSE)
```

The above diagram is the reference circuit diagram when connecting the SVGA-TFT LCD "LMTM080SVGNLA series" (8 inch), DLT800600AG104 series (10.4 inch) (DENSITRON), and "GKTS80SPAH series" (8 inch) (SGD).

・ Connection example to SVGA-TFT LCD (NEC)

from LCD Controller


```
               GND   R18   R17  +3.3V         CN8
                     10K   10K                1      1:D3+/GND
                                              2      2:D3-/GND
         U/D                                  3      3:DPS
                                              4      4:FRC
         TCLK+                                5      5:GND
         TCLK-                                6      6:CLK+
                                             7      7:CLK-
         TC+                                  8      8:GND
         TC-                                  9      9:D2+
                                              10     10:D2-
         TB+                                  11     11:GND
         TB-                                  12     12:D1+
                                              13     13:D1-
         TA+                                  14     14:GND
         TA-                                  15     15:D0+
                                              16     16:D0-
                                              17     17:GND
                                              18     18:MSL
                                              19     19:VCC
                                              20     20:VCC
                              GND        FI-SE20P-HFE(JAE)
```
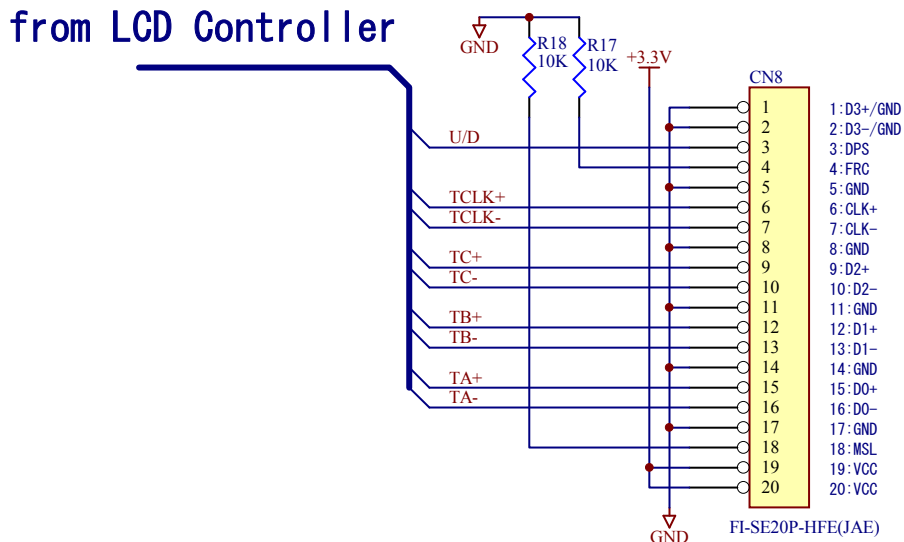
The above diagram is the reference circuit diagram when connecting the SVGA-TFT LCD "NL8060BC31 series" (NEC).

Kenic system

- Connection example to SVGA-TFT LCD (SHARP)

from LCD Controller

CN		
	1	1:GND
U/D	2	2:SELLVDS
	3	3:RL/UD
	4	4:GND
	5	5:RxIN3+
	6	6:RxIN3-
	7	7:GND
TCLK+	8	8:CK IN+
TCLK-	9	9:CK IN-
	10	10:GND
TC+	11	11:RxIN2+
TC-	12	12:RxIN2-
	13	13:GND
TB+	14	14:RxIN1+
TB-	15	15:RxIN1-
	16	16:GND
TA+	17	17:RxIN0+
TA-	18	18:RXIN0-
	19	19:GND
	20	20:GND
	21	21:VCC
	22	22:VCC
PWM	23	23:GND
	24	24:VBR
	25	25:XSTABY
	26	26:GND
BLEN	27	27:VDD
	28	28:VDD
	29	29:GND
	30	30:GND

+3.3V

+12V

R 10K

DT1 DTC124XUA

+12V

GND

GND

FI-XPB30SRL-HF11(JAE)
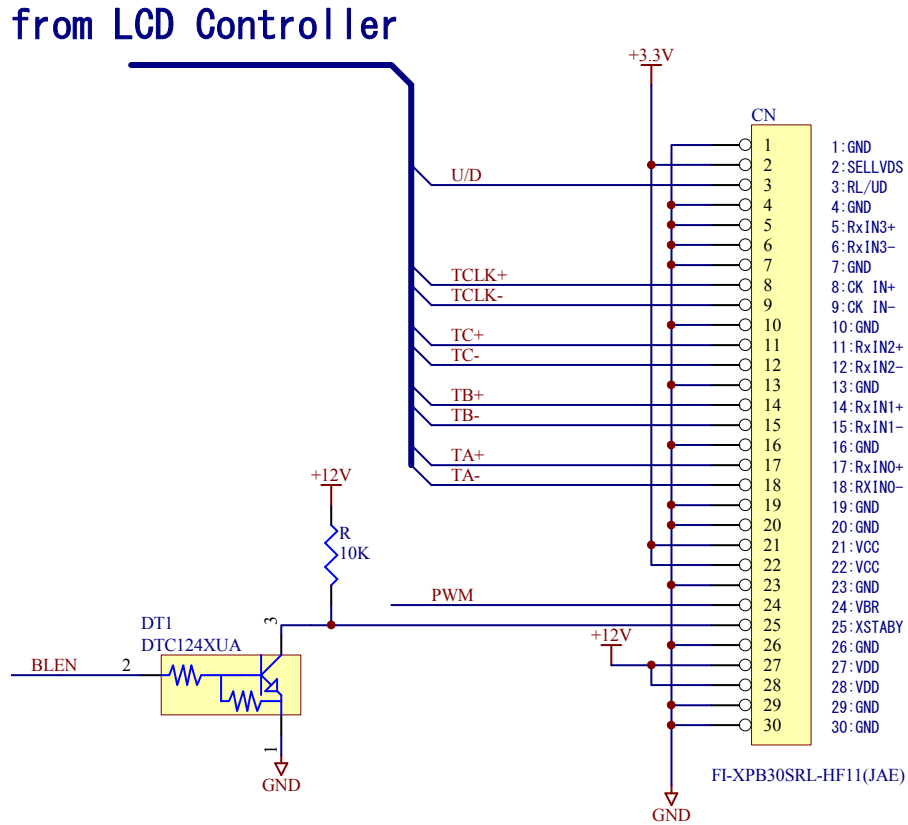
The above diagram is the reference circuit diagram when connecting the SVGA-TFT LCD "LQ121S1LG71 series" (SHARP).

Kenic system

・ About the LVDS Pattern

For the LVDS pattern wiring, be careful of the following points as much as possible.

- ・The wiring should use the fewest number of vias between the LCD controller and connector.
- ・When setting a via on one side of a differential pairing, also set a via on the other signal line, making the same state.
- ・Use isometric wiring between the LCD controller and connector.
- ・The distance between the LCD controller and connector should be as short as possible.
- ・Do not place a divided slit in the internal layer GND pattern of the LVDS signal.
- ・The wiring interval A between differential pairs should be at a minimum.
- ・The wiring interval between each pair should be A×2 or more.
- ・The LVDS and CMOS or TTL wiring interval should be A×3 or more.
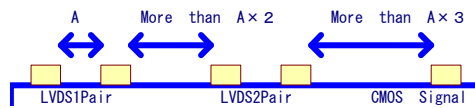
・ Signal mapping of the LVDS

The following diagram is a signal map of the LVDS signal output data.
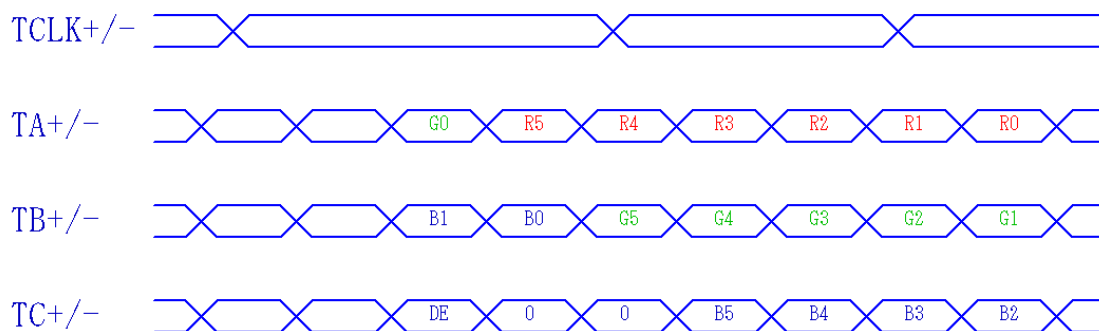
Kenic system

(5) Reference Circuit for Backlight I/F (reference)

・Reference circuit for LED backlight (Kenic System: KSLBC-4 (D4))
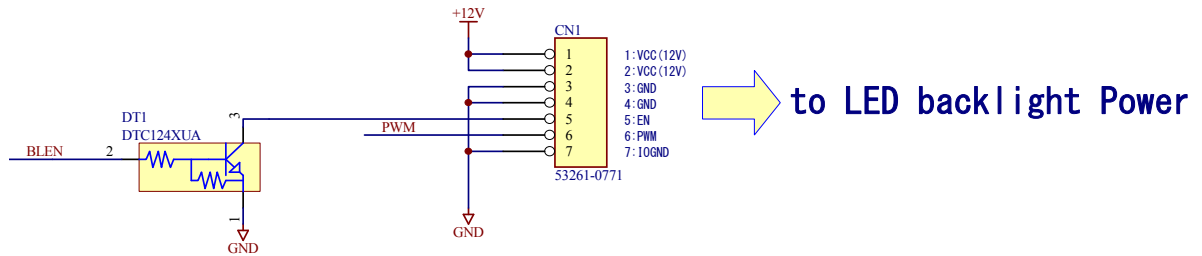
The above diagram is an example connection between the LED backlight power supply "KSLBC-4 (D4)" (Kenic system) (sold separately) and the LCD controller.

This LED backlight power supply can be used for the following LCDs: SVGA-TFT LCD "LMTM080SVGNLA series" (8 inch) (manufacturer: DENSITRON), GKTS80SPAH series" (8 inch) (SGD).

When the EN signal is open, the backlight is in the ON state. By connecting the BLEN signal outputted from the LCD controller to the open collector or digital transducer, ON/OFF for the backlight can be controlled.

Brightness of the backlight can be controlled by the PWM signal. The PWM frequency and ON width can be set by the register. For the setting method, refer to "11. About the registers". And, for the PWM input specification for the LED backlight power supply, refer to the LED backlight power supply specifications.

There are also LED backlight power supplys which are compatible with other LCDs. For more details, please make an inquiry to our sales staff.

Kenic system

5. Electrical Characteristics （DC, AC）, Access Timing Specifications

● Maximum Ratings

Item	Sign	Rating	Units
Power supply voltage	V_{CC}	-0.5~1.32	V
Power supply voltage	VCC AUX	-0.5~3.75	V
Power supply voltage	VCC J	-0.5~3.75	V
Power supply voltage	VCC PLL	-0.5~3.75	V
Output power supply voltage	VCC IO	-0.5~3.75	V
Voltage added to input or tri-state I/O		-0.5~3.75	V
Storage temperature (Ambiance)	T_{STG}	-65~+150	℃
Junction temperature	T_j	+125	℃

● Recommended Operating Conditions

Item	Sign	Min.	Max.	Units
Internal core power supply voltage	V_{CC}	1.14	1.26	V
Auxiliary power supply voltage	VCCAUX	3.135	3.465	V
PLL power supply voltage	VCCPLL	3.135	3.465	V
I/O driver power supply voltage	VCCIO0~2 and 4~7	3.135	3.465	V
	VCCIO3	2.375	2.625	V
IEEE1149.1 test access port power supply voltage	VCCJ	3.135	3.465	V
Junction temperature	Tj	0	85	℃
Ambient Operating temperature	Ta	0	60	℃

The LCD controller requires +1.2V （core power supply voltage）, +2.5V （VCCIO3 for LVDS）, and +3.3V （VCCIO except for VCCAUX, VCCPLL, VCCJ and VCCIO3）.

Kenic system

● Single end IO   DC Standard (at recommended operating conditions)

Item	Sign	Min.	Max.	Units
Input Hi voltage	V_{IH}	2.0	3.6	V
Input Low voltage	V_{IL}	-0.3	0.8	V
Output Hi voltage	V_{OH}	VCCIO -0.4		V
Output Low voltage	V_{OL}		0.4	V

● LVDS Differential IO   DC Standard (at recommended operating conditions)

Item	Sign	Test conditions	Min.	Rating	Max.	Units
Output differential voltage	V_{OD}	$(V_{OP}-V_{OM})$ RT=100Ω	250	350	450	mV
Change of V_{OD} between High and Low	ΔV_{OD}				50	mV
Output voltage offset	V_{OS}	$(V_{OP}+V_{OM})/2$ RT=100Ω	1.125	1.20	1.375	V
Change of V_{OS} between H and L	ΔV_{OS}				50	mV
Output short-circuit current	I_{SA}	$V_{OD}=0V$, shorting driver output to the GND.			24	mA
Output short-circuit current	I_{SAB}	$V_{OD}=0V$, shorting driver output mutually.			12	mA

● Approximate Current and Power Consumption

Power supply	Voltage [V]	Approximate current consumption [A]		Approximate power consumption ［W］	
		Standard	Max.	Standard	Max.
Vcc	1.2	0.1526	0.2729	0.1832	0.3274
VCCAUX[1]	3.3	0.0219	0.0242	0.0721	0.08
VCCPLL	3.3	0.0239	0.0239	0.079	0.079
VCCIO0~2,4~7	3.3	0.0525	0.0528	0.1731	0.1741
VCCIO3	2.5	0.0307	0.0307	0.07675	0.07675
VCCJ	3.3	0.0011	0.0011	0.0037	0.0037

1. For the power supply "VCCAUX", a peak of 0.085A may flow at start-up.

● Refresh Rate

Item	Sign	Standard	Units
Refresh rate		60	Hz

Kenic system

2) Write Cycle for the LCD Controller Host-CPU Interface
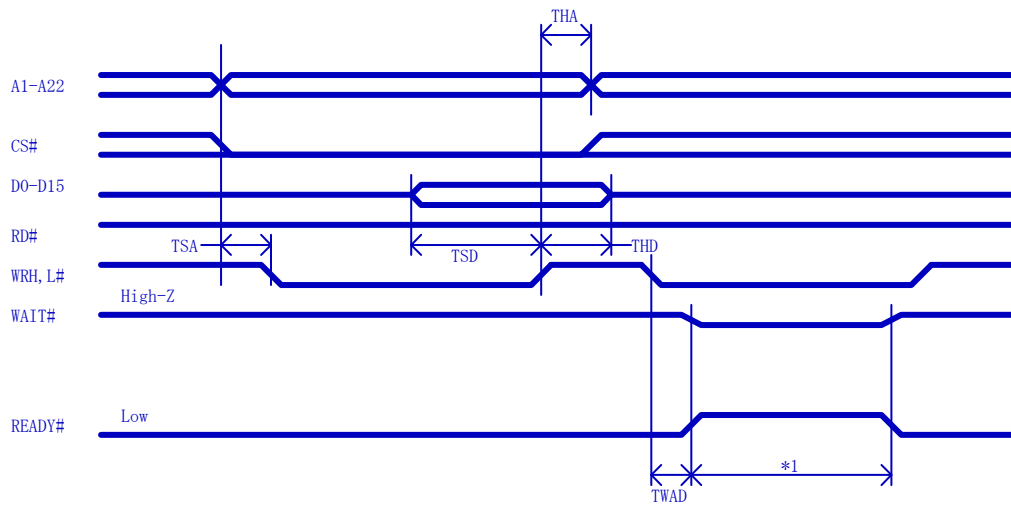
Sign	Item	Min.	Max.	Unit
TSA	Address setup	10	—	ns
THA	Address hold	12	—	ns
TSD	Data setup	5	—	ns
THD	Data hold	12	—	ns
TWAD	WAIT output delay	—	17	ns
*1	WAIT# (READY#) width	—	11000	ns

WAIT# and READY# signals are outputted under either of the following conditions.

・ When the time between the previous write signal rises and the next signal falls is 45 ns or less. (In the case of writing to the Color Palette Register and frame buffer memory.)

・ For this LCD controller, write data from the CPU to the frame buffer memory is written to the internal buffer (FIFO). The data written to the FIFO is read from the internal buffer when not reading display data from the frame buffer memory, and is written to the frame buffer.
The internal buffer has room for 1,024 pixels worth of data, but when the write data stored in the internal buffer exceeds the near-full state (data for 1,016 pixels), WAIT# (READY#) is outputted. At this time, when the write speed far exceeds the processing capacity of the LCD controller, the WAIT# (READY#) width becomes longer. However, the maximum values in the above table are only a worst case scenario; in fact, the possibility of it becoming this long is low.

Kenic system

3) Read Cycle for the LCD Controller Host-CPU Interface
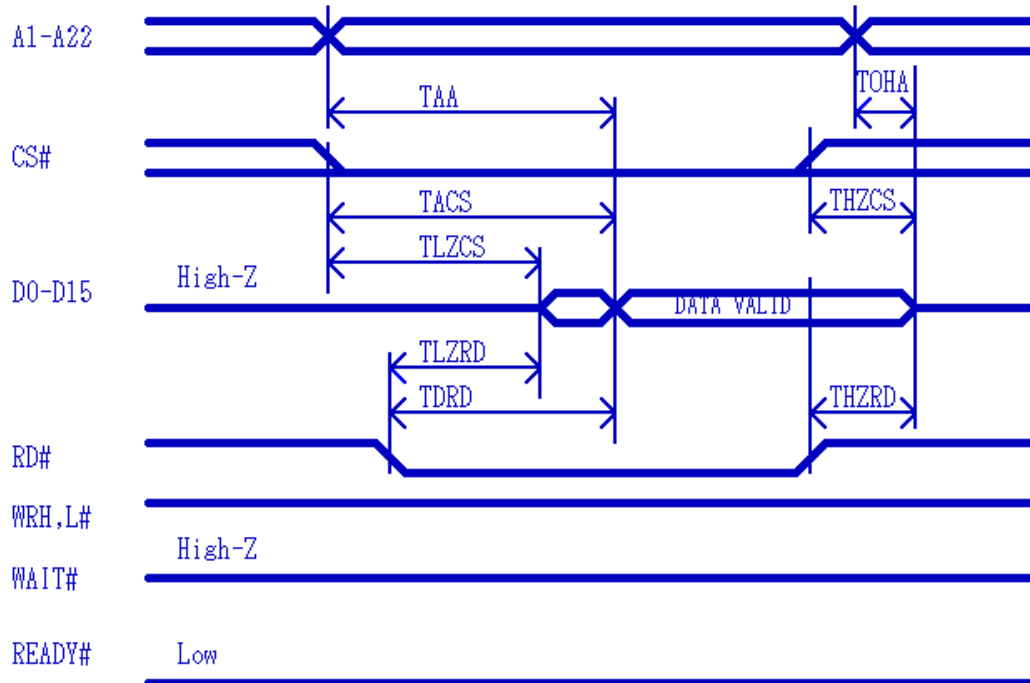
Sign	Item	Min.	Max.	Unit
TAA	Address access time	—	20	ns
TOHA	Output hold time	0	—	ns
TACS	Chip select access time	—	15	ns
TDRD	Read access time	—	15	ns
THZRD	Read disable output High-Z time	—	15	ns
TLZRD	Read enable output set time	0	—	ns
THZCS	Chip select disable output High-Z time	—	15	ns
TLZCS	Chip select enable output set time	0	—	ns

Caution) The LCD controller can be read only some registers, not be read the frame buffer memory.

Kenic system

4) CPU bus   Switching timing of I/O direction

· Image data transfer start time

```
BACK#         ───┐
                 └──────────────────────────────────

A0-A21
FROMCS#       ──── Input │ or  HIGH-Z ────╳──── Output ────
RD#

                 │←────────────────────→│
                       39nsec(min)
```
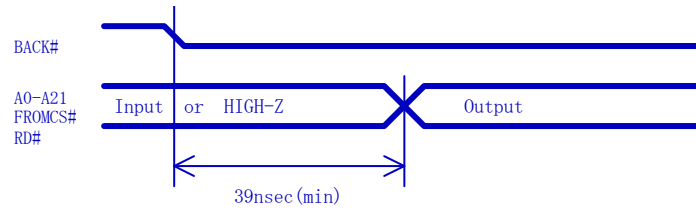
· Image data transfer finish time

```
BREQ#         ───┐
                 └──────────────────────────────────

A0-A21
FROMCS#       ──── Output ──╳── Input   or  HIGH-Z ────
RD#

                 │←──→│
                 10nsec(max)
```

Kenic system
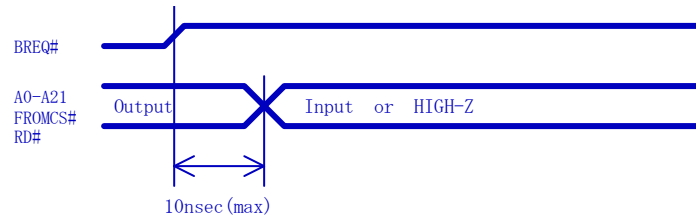
6.　Address Map

6-1 Address Map for the frame buffer memory

2,048 pixels (512 words×4 banks)

Area 1
64/4,096 color mode: Area 1×2 pages
65,536 color mode: Area 1×1 page

Area 2
64/4,096 color mode: Area 2×2 pages
65,536 color mode: Area 2×1 page

Area 3
64/4,096 color mode: Area 3×2 pages
65,536 color mode: Area 3×1 page

Area 4
64/4,096 color mode: Area 4×2 pages
65536 color mode: Area 4×1 page

1,024 pixels
1,024 pixels
1,024 pixels
1,024 pixels
1,024 pixels
4,096
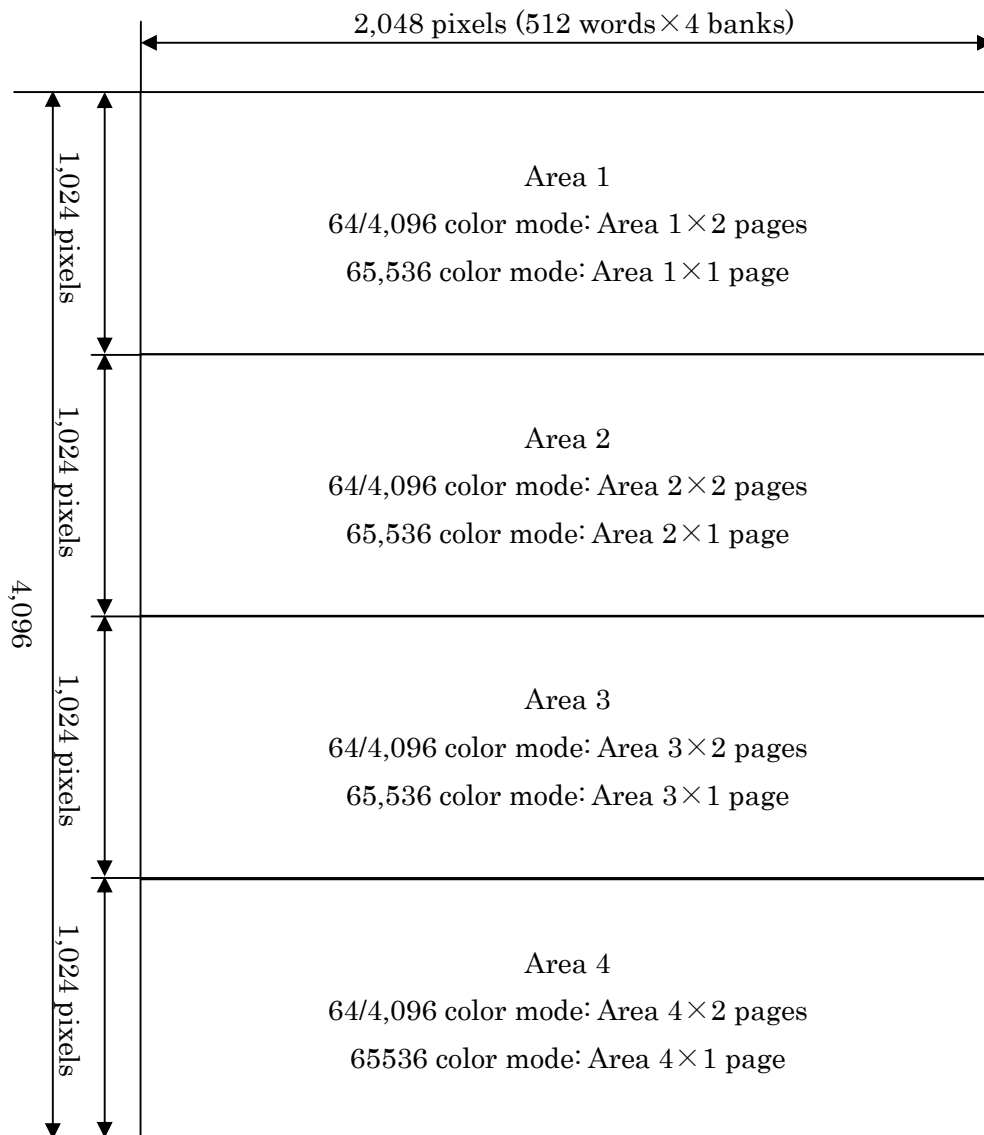
Diagram 6-1　Address Map for the frame buffer memory

The LCD controller is compatible with an SDR SDRAM of 4,096＊512 words＊4 banks. As in Diagram 6-1, the frame buffer memory is divided into four areas, with a screen resolution of 2,048 pixels (horizontal), 1,024 pixels (vertical) per area. With display and write area specified registers, the area that is displayed to the LCD and the area where the drawing data is written to can be selected.

Kenic system

In the 64/4,096 color mode, the frame buffer has room for 2 pages per area. With this, two-layer superimposed display (transparent display) within the same area is possible. In the 65,536 color mode, it becomes 1 page per area.

In addition, with the Display-start X-coordinate-setting Register and the Display-start Y-coordinate-setting Register, an image of 800*600 (SVGA) can be displayed from an arbitrary position in the area as shown in Diagram 6-2.

2,048 pixels (512 words×4 banks)

Display start coordinate (X, Y)

1,024 pixels

Display Area
800×600
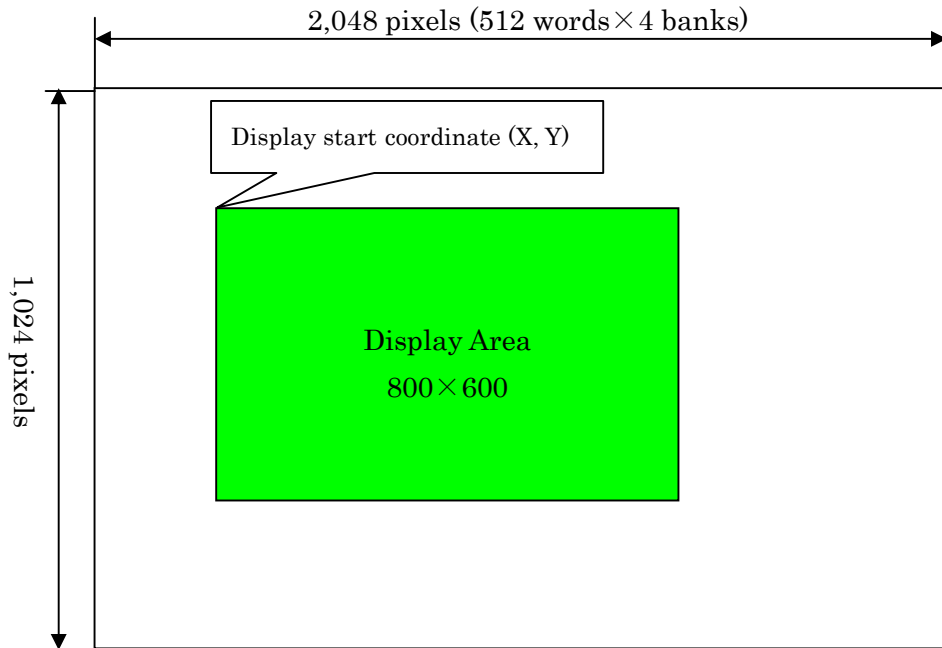
Diagram 6-2　Display Area

Kenic system

6-2 Address Map for the LCD controller

【KS-LTSV-SD (LVDS)】

000000H	**Frame Buffer** Area 1 (Area 2, 3, 4) : PAGE0 (PAGE1)
3FFFFFH	
400000H	Free
7FFF00H	
	Color Map Table
7FFF7FH	
7FFFC0H	Various Register
7FFFFFH	

The above is the address map for the LCD controller as viewed from the CPU. In 64 colors in 4,096 color mode, the frame buffer has 4 areas for 2 pages (PAGE0 and PAGE1). And, in 65,536 color mode, it has 4 areas.

The bank switching method is used to switch pages, and this is accomplished by setting control register 2 (DCR2). And, the area switching is accomplished by setting the register for display area and write area. Therefore, the address range of the frame buffer as viewed from the CPU is for one area.

Kenic system

7. Pixel Composition of the Screen

(1) 64 Colors in 4,096 Color Mode

In the 64 colors in 4,096 color mode, word access and/or byte access is possible.

For word access, set valid data in the lower byte of the 2 bytes from the address in the following diagram, and access the LCD controller. The data for the higher byte is ignored in the LCD controller.

Additionally, when conducting byte access, add one (+1) to the address in the following diagram, and access the LCD controller with an odd-numbered address.

```
(0,0)=0000H, (1,0)=0002H   ...                    ...  (2047, 0)=0FFEH
(0,1)=1000H, (1,1)=1002H   ...                    ...  (2047, 1)=1FFEH
(0,2)=2000H, (1,2)=2002H   ...                    ...  (2047, 2)=2FFEH



(0,1023)=3FF000H, (1,1023)=3FF002H   ...   ...   (2047, 1023)=3FFFFEH
```

Each pixel corresponds completely to each bit.

For this LCD controller, the frame buffer exists from (0, 0) to (2,047, 1,023) per area. However, the displayable area range is 800*600 beginning at the display start coordinate (coordinates set in the Display-start X-coordinate-setting Register and the Display-start Y-coordinate-setting Register.).

(2) 65,536 color mode

```
(0,0)=0000H, (1,0)=0002H   ...                    ...  (2047, 0)=0FFEH
(0,1)=1000H, (1,1)=1002H   ...                    ...  (2047, 1)=1FFEH
(0,2)=2000H, (1,2)=2002H   ...                    ...  (2047, 2)=2FFEH



(0,1023)=3FF000H, (1,1023)=3FF002H   ...   ...   (2047, 1023)=3FFFFEH
```

Each pixel corresponds completely to each bit.

Kenic system

For this LCD controller, the frame buffer exists from (0, 0) to (2,047, 1,023) per area. However, the displayable area range is 800*600 beginning at the display start coordinate (coordinates set in the Display-start X-coordinate-setting Register and the Display-start Y-coordinate-setting Register.).

Kenic system

8. Displayed Data

This LCD controller uses the color palette format. Firstly, the following is an explanation of this color palette format.

【About the color palette】

When displaying color, usually the color code is designated; for example, there are times when this color code is fixed, such as 02H for blue, 0CH for green, however, another method is when the value of 02H is not fixed to a color such as red but instead indicates that a value representing a color is being stored at that location. With this way, programmers can code more abstract software.

As such, the register housing the list of color addresses and the colors themselves is called the "color palette table."

For example, let's suppose the command "draw a BOX from (100, 100) to (200, 200) using color 03H" is written in the C language. The color indicated by 03H is at first aqua, but let's also say that afterwards we want to change the color to light green. In this case, we only have to change the color registered to 03H in the color palette, and the areas drawn using 03H will all change automatically. Even when the LCD can display only 64 colors, it is possible to select from 4,096 colors, allowing for a remarkably better visual quality.

(1) 64 Colors in 4,096 Color Mode

The displayed data to be written in each frame buffer need to have a set color palette code.

The access to the frame buffer is possible for both word access and byte access.

When writing data in word access, specify an even-numbered address for access. At this time, the data for the lower byte is valid.

When writing data in byte access, specify an odd-numbered address and access only the lower address.

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Image Memory Area

000000H~3FFFFEH (Higher bytes　D15~8)

Bit	15	14	13	12	11	10	9	8
Name	-	-	-	-	-	-	-	-
R/W	W	W	W	W	W	W	W	W
Initial value	-	-	-	-	-	-	-	-

(Caution) Initial value is indefinite.

Image Memory Area

000001H~3FFFFFH (Lower bytes　D7~0)

Bit	7	6	5	4	3	2	1	0
Name	M1	M0	P5	P4	P3	P2	P1	P0
R/W	W	W	W	W	W	W	W	W
Initial value	-	-	-	-	-	-	-	-

(Caution) Initial value is indefinite.

Pixel Control Bit　bits 7~6

M1	M0	Explanation
0	0	Normal display.
0	1	Transmission display.
1	0	Blink 1.
1	1	Blink 2.

(Caution)　These M1 and M0 bits function as part of a set with control register 1 (DCR).

Color Palette Table　bits 5~0

P5	P4	P4	P2	P1	P0	Explanation
0	0	0	0	0	0	The data housed in color map table 0~63 is displayed in advance.
0	0	0	0	0	1	
1	1	1	1	1	0	
1	1	1	1	1	1	

For the method to house color data for each color palette, refer to the "11. About the Registers" chapter.

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(2) 65,536 color mode

With the 65,536 color mode for DCR1, write 16-bit (RGB) data to the frame buffer memory in the following format.

Execute access to the frame buffer using only word access.

Per-byte access is not supported.

Image Memory Area

000000H~3FFFFEH (Higher bytes   D15~8)

Bit	15	14	13	12	11	10	9	8
Name	R4	R3	R2	R1	R0	G5	G4	G3
R/W	W	W	W	W	W	W	W	W
Initial value	-	-	-	-	-	-	-	-

Image Memory Area

000001H~3FFFFFH (Lower bytes   D7~0)

Bit	7	6	5	4	3	2	1	0
Name	G2	G1	G0	B4	B3	B2	B1	B0
R/W	W	W	W	W	W	W	W	W
Initial value	-	-	-	-	-	-	-	-

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9. Drawing Function

This LCD controller includes the following drawing functions.

(1) Line Drawing Function
(2) Arbitrary Rectangle Fill-in Function

9-1 Line Drawing Function

By using this function, arbitrary lines (vertical, horizontal, and diagonal) can be drawn at high-speed.
When drawing a line as in Diagram 9-1, after setting the starting point coordinates (X1, Y1), the ending point coordinates (X2, Y2), and the color to the register (Regarding registers, refer to "11. About the Registers".), the line drawing function is performed in the Line-drawing Start-setting Register.
As the size comparison of the starting and ending point coordinates is executed inside the LCD controller, for the Host-CPU side software, register settings can be conducted without worrying about the size comparison. Also, the coordinate register is 2 bytes. When setting a value larger than the area size (2,048×1,024 pixels), beware that the display can become strange.
During the line drawing process, avoid accessing the frame buffer memory from the CPU, performing other drawing functions (Hard Fill, Arbitrary Rectangle Fill-in Function, Image Data Transfer Function), or line drawing. During the line drawing process, place a BUSY flag of the Hard Fill Status Register. Check for this flag and confirm that the operation has completed before accessing the frame buffer memory or executing the next drawing function. Additionally, at the completion of the operation, a one-shot signal of the ACTIVE LOW is outputted from the INTOUT signal of the LCD controller (The pulse width is about 1μSEC.). By connecting this signal to the IRQ port of the CPU, the CPU can detect the completion of the operation by interruption.
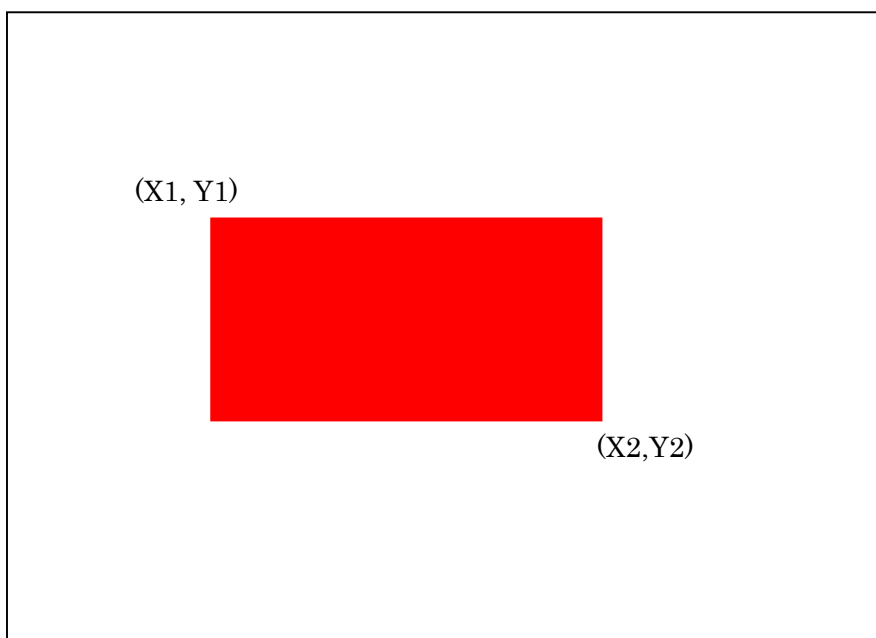In the 64/4,096 color mode, the drawing is performed in the display area and write area specified in the write area-specified register, and in a page specified for the DCR2 register.

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In the 65,536 color mode, the data is written to the displayed area and the write area specified in the write area-specified register.

Diagram 9-1   About Line Drawing

9-2   Arbitrary Rectangle Fill-in Function

By using this function, arbitrary rectangle fill-in can be drawn at high-speed.

When drawing a rectangle fill-in as in Diagram 9-2, after setting the starting point coordinates (X1, Y1), the ending point coordinates (X2, Y2), and the color to the register (Regarding registers, refer to "12. About the Registers".), the rectangle fill-in function is performed in the Rectangle Fill-in Start Register.

As the size comparison of the starting and ending point coordinates is executed inside the LCD controller, for the Host-CPU side software, register settings can be conducted without worrying about the size comparison. Also, the coordinate register is 2 bytes. When setting a value larger than the area size (2,048×1,024 pixels), beware that the display can become strange, it will take time before the drawing completes.

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During the rectangle fill-in process, avoid accessing the frame buffer memory from the CPU, performing other drawing functions (Hard Fill, Line Drawing Function, Image Data Transfer Function), or rectangle fill-in. During the rectangle fill-in process, place a BUSY flag of the Hard Fill Status Register. Check for this flag and confirm that the operation has completed before accessing the frame buffer memory or executing the next drawing function. Additionally, at the completion of the operation, a one-shot signal of the ACTIVE LOW is outputted from the INTOUT signal of the LCD controller (The pulse width is about 1μSEC.). By connecting this signal to the IRQ port of the CPU, the CPU can detect the completion of the operation by interruption.

Diagram 9-2   About Rectangle Fill-in

In the 64/4,096 color mode, the drawing is performed in the display area and write area specified in the write area-specified register, and in a page specified for the DCR2 register.

In the 65,536 color mode, the data is written to the displayed area and the write area specified in the write area-specified register.

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10. Image Data Transfer Function

The "Image Data Transfer Function" is a function that reads arbitrary image data from the FROM for images connected to the CPU, writes to the frame buffer, and displays an image on arbitrary coordinates. The LCD controller outputs the bus release signal to the CPU in order to read the data from the FROM for images connected to the CPU, and then checks the release of the bus before reading image data from the FROM for images. Therefore, the CPU is unable to access the external bus during this time.

Only necessary information has to be set in the following registers for the LCD controller to transfer image data automatically (Regarding registers, refer to "11. About the Registers.").

- Image-display Start-position X-coordinate-setting Register
- Image-display Start-position Y-coordinate-setting Register
- Leading-address-setting Register for the Image Data Storage Location
- Image-data Display-size Width-setting Register
- Image-data Display-size Line-number-setting Register
- Image Control Register

For example, when displaying image data stored in the FROM for images to the display coordinates (X1, Y1) as shown in Diagram 10-1, set the leading address where the image data is stored in the Leading-address-setting Register for the Image Data Storage Location, and set the display coordinates (X1, Y1) in the Image-display Start-position X-coordinate-setting Register and the Image-display Start-position Y-coordinate-setting Register. Next, set the display size of the image data (width, line number) in the Image-data Display-size Width-setting Register and the Image-data Display-size Line-number-setting Register. When executing the transfer in the Image Control Register, the LCD controller transfers the image data automatically, and the display is performed. While transferring image data, the CPU is unable to use the external bus.

After completing the transfer, the LCD controller stops the bus open

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command to the CPU, and a one-shot signal of the $\overline{\text{ACTIVE LOW}}$ is outputted from the INTOUT pin (The pulse width is about 1μSEC.). Connect this signal to the IRQ port of the CPU; confirm the completion of the transfer before the CPU accesses the external bus.

In addition, use this function in the 65,536 color mode, as the displayed colors become strange when operating in the 64/4,096 color mode.

Image data is written to the displayed area and the write area specified in the write-area-specified register.
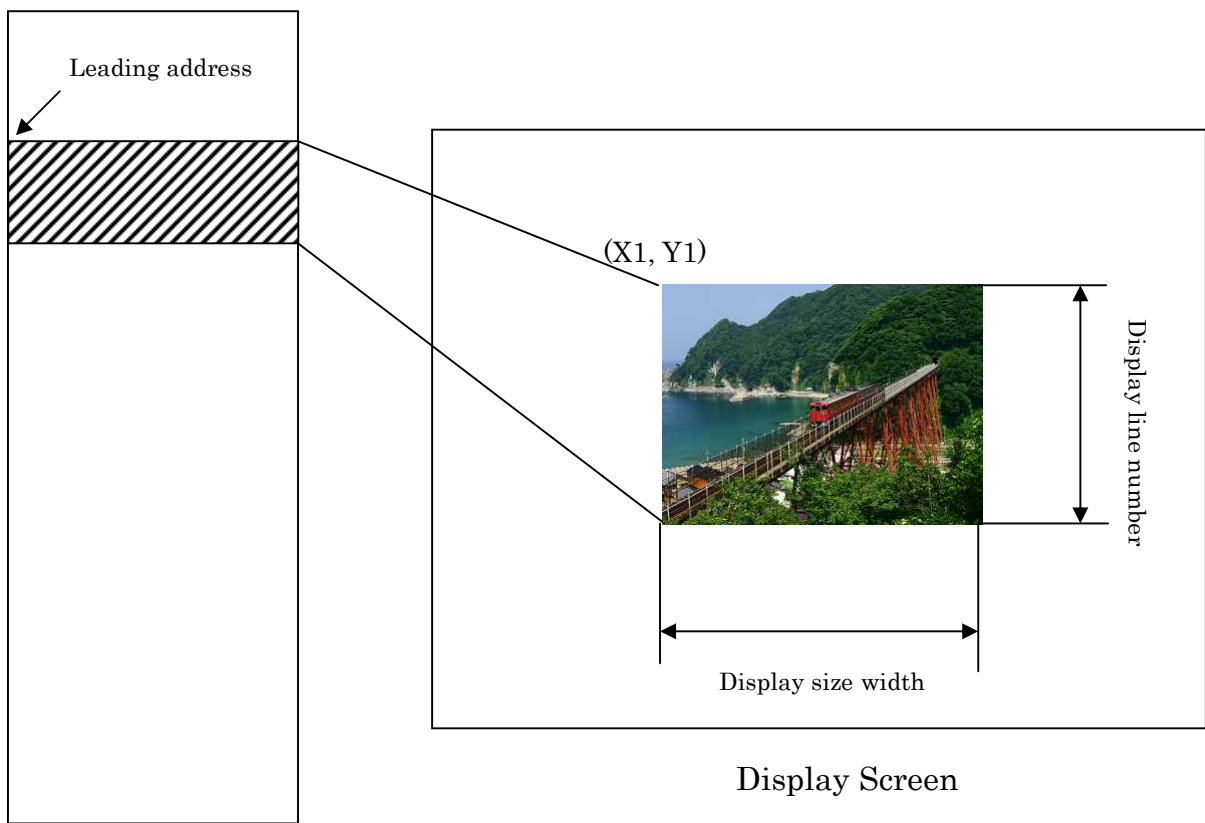
Diagram 10-1　Image Data Transfer Image

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10-1　Accessing the FROM for images

When the image data transfer is stopped, it is possible to access the FROM for images from the CPU, and image data can be written.
For the amount of image data that can be stored in the FROM for images when its capacity is 64Mbytes (512Mbits), with a QVGA (320*240 pixels) image the size is as follows:

320*240*2Bytes＝153.6kBytes

Therefore, in the FROM for images, the following number of images can be saved.

64Mbytes/153.6kBytes＝about 416 images

In VGA size (640*480 pixels),

640*480*2 Bytes＝614.4kBytes

Thus, in the FROM for images, the following number of images can be saved.

64Mbytes/614.4kBytes＝about 104 images

The LCD controller provides 3-bit output pins A24~A22: FA24 (No.206 pin), FA23 (No. 207 pin), and FA22 (No. 1 pin). As these pins are output pins, avoid connecting to the address signal line from the CPU. Connect to the address pin of the FROM for images from this pin. The 3-bit signal of A24~A22 outputs the contents of the FROM for images address register as-is.

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10-2   Transfer Time of Image Data and Video Speed

The time required to read an image with the dimensions of 320*240 from the FROM for images and write to the frame buffer memory is as follows.

$$320×240×182.5nsec＝14.02msec$$

Therefore, video playback of 30 frames per second (about 33.3 msec cycle) is possible. Moreover, for the dimensions of 640*480 (in case of VGA size),

$$640×480×182.5nsec＝56.06msec$$

Therefore, video playback of 15 frames per second (about 66.7msec cycle) is possible.

10-3   About Video

By using the following method (Example: Image size is 640*480, when screen is refreshed at 15 frames per second), video can be played back smoothly.

(1)   Connect the VSYNC signal outputted from the LCD controller to the interrupt pin input of the CPU.
(2)   Fill in an area (area 1, 2) with hard fill in a single color.
(3)   If VSYNC interruption is detected, make area 1 the write area and area 2 the display area, and transfer the first image.
(4)   With VSYNC interruption, after 4 frames (1 frame: about 16.7msec), make area 1 the display area and area 2 the write area, and transfer the next image.
       At this time, the image transferred in (3) is displayed.
(5)   With VSYNC interruption, after 4 frames (1 frame: about 16.7msec), make area 1 the write area and area 2 the display area, and transfer the next image.
       At this time, the image transferred in (4) is displayed.
(6)   Smooth animation can be performed by repeating (4) and (5).

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10-4　　During Image Data Transfer

While transferring image data, the CPU bus is released, and because the LCD controller takes over the CPU bus, the CPU is unable to access the external bus during the transfer.

In addition, be aware that depending on the CPU type, there are those which practically stop processing during the bus release.

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11. About the Registers

(1) Register for the Color Palette
    Addresses   7FFF00H~7FFF7FH

There are 64 color palettes, and each can be set as 12-bit (4,096 colors).
The palette number must be set for drawing.

The write to the color palette register is possible for both in units of byte and word. In word access, the higher side of the data bus is G3~0, B3~0, the lower side of the data bus is R3~0.

Color Palette Address List

Bit order	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
Color data format	-	-	-	-	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0
Palette 0	7FFF01H								7FFF00H							
Palette 1	7FFF03H								7FFF02H							
Palette 2	7FFF05H								7FFF04H							
	• • • •															
Palette 61	7FFF7BH								7FFF7AH							
Palette 62	7FFF7DH								7FFF7CH							
Palette 63	7FFF7FH								7FFF7EH							

Example) Color Palette 63

Address   7FFF7EH (Even Address   G, B)

Bit	7	6	5	4	3	2	1	0
Name	G3	G2	G1	G0	B3	B2	B1	B0
R/W	W	W	W	W	W	W	W	W
Initial value	-	-	-	-	-	-	-	-

Address   7FFF7FH (Odd Address   R)

Bit	7	6	5	4	3	2	1	0
Name					R3	R2	R1	R0
R/W	W	W	W	W	W	W	W	W
Initial value	-	-	-	-	-	-	-	-

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(2) FROM for Images Address Register (For bank switching)

Address   7FFFC0H

Bit	7	6	5	4	3	2	1	0
Name	—	—	FA24	FA23	FA22	—	—	—
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

Use this register when accessing a high-capacity (512Mbit) FROM for images from the CPU and the high-order bit address of the CPU is insufficient.

Bit information set to bits 5, 4, 3 of this register is outputted from the No. 206, 207 and No.1 pins of the LCD controller.

The register can be written to by byte or word access. For word access, set the data in the high-order byte (D15~8).

(3) Image-display Start-position X-coordinate-setting Register

Address   7FFFC2H

Bit	15	14	13	12	11	10	9	8
Name	-	-	-	-	-	X(10)	X(9)	X(8)
R/W	-	-	-	-	-	W	W	W
Initial value	-	-	-	-	-	0	0	0

Address   7FFFC3H

Bit	7	6	5	4	3	2	1	0
Name	X(7)	X(6)	X(5)	X(4)	X(3)	X(2)	X(1)	X(0)
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

This register sets the X-coordinate of the image display starting point. The setting range is 0~2,047.

The limit is not applied on the FPGA side.

The register can be written to by byte or word access.

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(4) Image-display Start-position Y-coordinate-setting Register

Address   7FFFC4H

Bit	15	14	13	12	11	10	9	8
Name	-	-	-	-	-	-	Y(9)	Y(8)
R/W	-	-	-	-	-	-	W	W
Initial value	-	-	-	-	-	-	0	0

Address   7FFFC5H

Bit	7	6	5	4	3	2	1	0
Name	Y(7)	Y(6)	Y(5)	Y(4)	Y(3)	Y(2)	Y(1)	Y(0)
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

This register sets the Y-coordinate of the image display starting point.
The setting range is 0~1,023.
The limit is not applied on the FPGA side.
The register can be written to by byte or word access.

(5) Leading-address-setting Register for the Image Data Storage Location

Address   7FFFC6H

Bit	15	14	13	12	11	10	9	8
Name	-	-	-	-	-	-	-	FA(24)
R/W	-	-	-	-	-	-	-	W
Initial value	-	-	-	-	-	-	-	0

Address   7FFFC7H

Bit	7	6	5	4	3	2	1	0
Name	FA(23)	FA(22)	FA(21)	FA(20)	FA(19)	FA(18)	FA(17)	FA(16)
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

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Address   7FFFC8H

Bit	15	14	13	12	11	10	9	8
Name	FA(15)	FA(14)	FA(13)	FA(12)	FA(11)	FA(10)	FA(9)	FA(8)
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

Address   7FFFC9H

Bit	7	6	5	4	3	2	1	0
Name	FA(7)	FA(6)	FA(5)	FA(4)	FA(3)	FA(2)	FA(1)	FA(0)
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

This register sets the leading address of the FROM where image data is stored. The setting range is 0H~01FFFFFFH.

The register can be written to by byte or word access. In word access, write using two steps: "7FFFC6H ~ 7FFFC7H" and "7FFFC8H ~ 7FFFC9H".

(6) Image-data Display-size Width-setting Register

Address   7FFFCAH

Bit	15	14	13	12	11	10	9	8
Name	-	-	-	-	XH(11)	XH(10)	XH(9)	XH(8)
R/W	-	-	-	-	W	W	W	W
Initial value	-	-	-	-	0	0	0	0

Address   7FFFCBH

Bit	7	6	5	4	3	2	1	0
Name	XH(7)	XH(6)	XH(5)	XH(4)	XH(3)	XH(2)	XH(1)	XH(0)
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

This register sets the display width of image to display.

The setting range is 1~2,048.

The limit is not applied on the FPGA side.

The register can be written to by byte or word access.

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（7） Image-data Display-size Line-number-setting Register

Address 7FFFCCH

Bit	15	14	13	12	11	10	9	8
Name	-	-	-	-	-	YV(10)	YV(9)	YV(8)
R/W	-	-	-	-	-	W	W	W
Initial value	-	-	-	-	-	0	0	0

Address 7FFFCDH

Bit	7	6	5	4	3	2	1	0
Name	YV(7)	YV(6)	YV(5)	YV(4)	YV(3)	YV(2)	YV(1)	YV(0)
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

This register sets the display line number of image to display.

The setting range is 1~1,024.

The limit is not applied on the FPGA side.

The register can be written to by byte or word access.

（8） Image Control Register

Address 7FFFCEH（Write side）

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	ST
R/W	-	-	-	-	-	-	-	W
Initial value	-	-	-	-	-	-	-	0

This register sets the transfer start command for image data.

Bit 0   carries out the start instruction for image data transfer.

ST	Explanation
1	Transfer of image data is started.
0	This is an initial value or is returned to 0 after starting operation.

When the transfer of image data is completed, a one-shot signal of the

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ACTIVE LOW is outputted from the INTOUT signal of the LCD controller. The pulse width is about 1μSEC. With IRQ interruption processing, the CPU side can setup and start transfer of the next image data.

(9) Drawing X-coordinates-starting-point Setting Register

Address 7FFFD0H

Bit	15	14	13	12	11	10	9	8
Name	-	-	-	-	-	X(10)	X(9)	X(8)
R/W	-	-	-	-	-	W	W	W
Initial value	-	-	-	-	-	0	0	0

Address 7FFFD1H

Bit	7	6	5	4	3	2	1	0
Name	X(7)	X(6)	X(5)	X(4)	X(3)	X(2)	X(1)	X(0)
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

This register sets the X starting point coordinates of the drawing data.

The setting range is 0~2,047.

The limit is not applied on the FPGA side.

The register can be written to by byte or word access.

It is the same as the Arbitrary Rectangle Fill-in and Line-drawing Functions.

(10) Drawing Y-coordinates-starting-point Setting Register

Address 7FFFD2H

Bit	15	14	13	12	11	10	9	8
Name	-	-	-	-	-	-	Y(9)	Y(8)
R/W	-	-	-	-	-	-	W	W
Initial value	-	-	-	-	-	-	0	0

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Address 7FFFD3H

Bit	7	6	5	4	3	2	1	0
Name	Y(7)	Y(6)	Y(5)	Y(4)	Y(3)	Y(2)	Y(1)	Y(0)
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

This register sets the Y starting point coordinates of the drawing data.

The setting range is 0~1,023.

The limit is not applied on the FPGA side.

The register can be written to by byte or word access.

It is the same as the Arbitrary Rectangle Fill-in and Line-drawing Functions.

(11) Drawing X-coordinates-ending-point Setting Register

Address 7FFFD4H

Bit	15	14	13	12	11	10	9	8
Name	-	-	-	-	-	X(10)	X(9)	X(8)
R/W	-	-	-	-	-	W	W	W
Initial value	-	-	-	-	-	0	0	0

Address 7FFFD5H

Bit	7	6	5	4	3	2	1	0
Name	X(7)	X(6)	X(5)	X(4)	X(3)	X(2)	X(1)	X(0)
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

This register sets the X ending point coordinates of the drawing data.

The setting range is 0~2,047.

The limit is not applied on the FPGA side.

The register can be written to by byte or word access.

It is the same as the Arbitrary Rectangle Fill-in and Line-drawing Functions.

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(12) Drawing Y-coordinates-endting-point Setting Register

Address 7FFFD6H

Bit	15	14	13	12	11	10	9	8
Name	-	-	-	-	-	-	Y(9)	Y(8)
R/W	-	-	-	-	-	-	W	W
Initial value	-	-	-	-	-	-	0	0

Address 7FFFD7H

Bit	7	6	5	4	3	2	1	0
Name	Y(7)	Y(6)	Y(5)	Y(4)	Y(3)	Y(2)	Y(1)	Y(0)
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

This register sets the Y ending point coordinates of the drawing data.

The setting range is 0~1,023.

The limit is not applied on the FPGA side.

The register can be written to by byte or word access.

It is the same as the Arbitrary Rectangle Fill-in and Line-drawing Functions.

(13) Drawing Color-specified Register

・ 64/4,096 color mode

In 64/4,096 color mode, the palette number must be set.

Address 7FFFD9H

Bit	7	6	5	4	3	2	1	0
Name	M1	M0	P5	P4	P3	P2	P1	P0
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

・ 65,536 color mode

Address 7FFFD8H

Bit	15	14	13	12	11	10	9	8
Name	R4	R3	R2	R1	R0	G5	G4	G3
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

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Address 7FFFD9H

Bit	7	6	5	4	3	2	1	0
Name	G2	G1	G0	B4	B3	B2	B1	B0
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

This register sets the display colors of the drawing data.

The register can be written to by byte or word access.

It is the same as the Arbitrary Rectangle Fill-in and Line-drawing Functions and Hard Fill.

(14) Rectangle Fill-in Start Register

Address 7FFFDAH

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	ST
R/W	-	-	-	-	-	-	-	W
Initial value	-	-	-	-	-	-	-	0

This register sets the start command for rectangle fill-in.

Bit 0   carries out the start instruction for rectangle fill-in.

ST	Explanation
1	Rectangle fill-in is started.
0	This is an initial value or is returned to 0 after starting operation.

Caution) At the completion of the operation, a one-shot signal of the ACTIVE LOW is outputted from the INTOUT signal of the LCD controller (The pulse width is about 1μSEC.).

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(15) Line Drawing Start Register

Address 7FFFDCH

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	ST
R/W	-	-	-	-	-	-	-	W
Initial value	-	-	-	-	-	-	-	0

This register sets the start command for line drawing.

Bit 0   carries out the start instruction for the line drawing.

ST	Explanation
1	Line drawing is started.
0	This is an initial value or is returned to 0 after starting operation.

Caution) At the completion of the operation, a one-shot signal of the ACTIVE LOW is outputted from the INTOUT signal of the LCD controller (The pulse width is about 1μSEC.).

(16) Display-start X-coordinate-setting Register

Address 7FFFDEH

Bit	15	14	13	12	11	10	9	8
Name	-	-	-	-	-	X(10)	X(9)	X(8)
R/W	-	-	-	-	-	W	W	W
Initial value	-	-	-	-	-	0	0	0

Address 7FFFDFH

Bit	7	6	5	4	3	2	1	0
Name	X(7)	X(6)	X(5)	X(4)	X(3)	X(2)	X(1)	X(0)
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

This register sets the display start X-axis coordinates.
The setting range is 0~2,047.

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The limit is not applied on the FPGA side.

The register can be written to by byte or word access.

The content of this register is reflected from the time it is written by the CPU when the next display frame is started.

(17) Display-start Y-coordinate-setting Register

Address 7FFFFE0H

Bit	15	14	13	12	11	10	9	8
Name	-	-	-	-	-	-	Y(9)	Y(8)
R/W	-	-	-	-	-	-	W	W
Initial value	-	-	-	-	-	-	0	0

Address 7FFFFE1H

Bit	7	6	5	4	3	2	1	0
Name	Y(7)	Y(6)	Y(5)	Y(4)	Y(3)	Y(2)	Y(1)	Y(0)
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

This register sets the display start Y-axis coordinates.

The setting range is 0~1,023.

The limit is not applied on the FPGA side.

The register can be written in byte or word access.

The content of this register is reflected from the time it is written by the CPU when the next display frame is started.

(18) Display Area and Write Area-Specified Register

Address 7FFFFE2H

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	DISP AREA1	DISP AREA0	WR AREA1	WR AREA0
R/W	-	-	-	-	W	W	W	W
Initial value	-	-	-	-	0	0	0	0

This register specifies the display and write areas in the frame buffer

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memory area.

The drawing data from the CPU, the drawing functions (Line-drawing, Rectangle Fill-in, and Image Data Transfer), and the hard fill data are written to a specified write area.

Bits 3~2

DISP AREA1	DISP AREA0	Explanation
0	0	Display the area 1
0	1	Display the area 2
1	0	Display the area 3
1	1	Display the area 4

Bits 1~0

WR AREA1	WR AREA0	Explanation
0	0	Write to the area 1
0	1	Write to the area 2
1	0	Write to the area 3
1	1	Write to the area 4

(19) X-coordinate Obtained-data Register for the Touch Panel

Address 7FFFF0H

Bit	15	14	13	12	11	10	9	8
Name	ADB7	ADB6	ADB5	ADB4	ADB3	ADB2	ADB1	ADB0
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

Address 7FFFF1H

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

KS-R8TPC has an 8-bit A/D conversion function; this conversion result is received by KS-LTSV-SD (LVDS) and housed to the register automatically. The data is housed to the higher 8-bits. Sampling speed is continuously performed at around 5mS~8mS, and read from the above

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register is always possible. The data can be read from the higher byte. The lower byte is always read 0.

With this function, an interface without excessive hardware (analog joystick, analog touch panel, or other analog sensors) is possible.

(20) Y-coordinate Obtained-data Register for the Touch Panel

Address 7FFFF2H

Bit	15	14	13	12	11	10	9	8
Name	ADB7	ADB6	ADB5	ADB4	ADB3	ADB2	ADB1	ADB0
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

Address 7FFFF3H

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

The function of the register is like X-coordinate obtained-data register for the touch panel can also read A/D conversion results. The data can be read from the higher byte. The low byte is always read 0.

(21) PWM Frequency Setting Register

Address 7FFFF6H

Bit	15	14	13	12	11	10	9	8
Name	PF15	PF14	PF13	PF12	PF11	PF10	PF9	PF8
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	1	0	0	1	0	1

Address 7FFFF7H

Bit	7	6	5	4	3	2	1	0
Name	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
R/W	W	W	W	W	W	W	W	W
Initial value	0	1	1	1	0	1	0	1

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This register sets the frequency of the PWM. Use the following formula to set the value of the register.

Register value＝(Φ/ PWM frequency)－1
Φ＝4.79525MHz

For example, if you want to set the PWM frequency to "500Hz",

Register value＝(4.79525MHz /500Hz)－1
＝9,589 (decimal places truncated)

Set "9,589" in the register.

The initial value of the register is 9,589 and the PWM frequency is 500Hz.

The setting range is from 1 (PWM frequency: about 2.4MHz) to 65,534 (PWM frequency: about 73Hz).

(22) PWM　ON Width Setting Register

Address 7FFFF8H

Bit	15	14	13	12	11	10	9	8
Name	PW15	PW14	PW13	PW12	PW11	PW10	PW9	PW8
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	1	0	0	1	0	1

Address 7FFFF9H

Bit	7	6	5	4	3	2	1	0
Name	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0
R/W	W	W	W	W	W	W	W	W
Initial value	0	1	1	1	0	1	1	0

This register sets the ON width of the PWM. Use the following formula to set the value of the register.

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Register value = ((PWM frequency setting register + 1)*ON width [%])/100

For example, if you want to set the PWM frequency to "500Hz", and set width to "100%",

Register value＝((9,589+1)*100%)/100

＝9,590 (decimal places truncated)

Set "9,590" in the register.

The initial value of the register is "9,590" and the PWM frequency is 500Hz, and the ON width is 100%.

(23) Control Register 3 (DCR3)

Address 7FFFFBH (Write side)

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	U/D	R/L	BLI
R/W	-	-	-	-	-	W	W	W
Initial value	-	-	-	-	-	0	0	1

DCR3 performs display control for the LCD, and ON/OFF control for the backlight.

Bits 2~1 controls the display direction.

Register Setting Value		Display Switching Output Signal		Display orientation Explanation
U/D	R/L	U/D	R/L	
0	0	0	0	
0	1	0	1	Refer to the LCD data sheet.
1	0	1	0	
1	1	1	1	

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Bit 0

Register Setting	Output Signal	Explanation
BLI	BLEN	
0	1	Backlight off
1	0	Backlight on

・When setting the BLI bit "0", PWM output is fixed in LOW.

(24) Control Register 1 (DCR1)

Address 7FFFFCH (Write side)

Bit	7	6	5	4	3	2	1	0
Name	MODE	BLK2	BLK1	PEE	BK1	BK0	FR1	FR0
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

DCR1 sets the foreground/background of the frame buffer (2 pages), controls transmission display, controls Blink 1 and 2, and controls ON/OFF display.

Bit 7

MODE	Explanation
0	4,096 colors in 64 color mode.
1	65,536 color mode.

Bits 6~5

BLK2	BLK1	Explanation
0		Blink 2 inactive.
1		Blink 2 active.
	0	Blink 1 inactive.
	1	Blink 1 active.

(Note) Blink 2 can blink at a higher speed than blink 1.

　　　Blinking cycle for each LCD controller is as follows.

　　　Blink 1 blinking cycle　・・・　About 1 second
　　　Blink 2 blinking cycle　・・・　About 0.5 second

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Bit 4

PEE	Explanation
0	Transmission display inactive.
1	Transmission display active.

（Caution） Only in the 4,096 color mode. Transparent display is possible between pages in the same area. Transparent display of pages in different areas is not possible.

Bits 3~2

BK1	BK0	Explanation
0	0	The background page is Page 0.
0	1	The background page is Page 1.
1	0	Inactive setting.
1	1	Inactive setting.

Bits 1~0

FR1	FR0	Explanation
0	0	The foreground page is Page 0.
0	1	The foreground page is Page 1.
1	0	Inactive setting.
1	1	Inactive setting.

（25） Control Register 2 　（DCR2）

Address 7FFFFDH（Write side）

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	WFB1	WFB0
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

DCR2 sets the write page (2 pages) in the area. The drawing data from the CPU, the drawing data from inside of the LCDC, and the hard fill data is written to the specified write page. These settings are effective only in the 64/4,096 color mode.

The drawing data from inside of the LCDC includes the following:

・ Line drawing
・ Arbitrary Rectangle Fill-in

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Bits 1~0

WFB1	WFB0	Explanation
0	0	Write page is set to page 0.
0	1	Write page is set to page 1.
1	0	Inactive setting.
1	1	Inactive setting.

Caution) In the 65,536 color mode, write is performed to Page0 and Page1 without regard to the setting of this bit.

(26) Hard Fill Command Register (CFCR)

Address 7FFFFFH

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	BUSY
R/W	-	-	-	-	-	-	-	R/W
Initial value	-	-	-	-	-	-	-	0

In 64/4,096 color mode, with the palette number housed in the drawing color specified register, color data from the color palette register is selected, and the data is used to fill the frame buffer for the page set in the WFB bit of DCR2.

In 65,536 color mode, with the displayed color housed in the drawing color-specified register, the frame buffer is filled.

And, it is performed to the write area specified in Display Area and Write Area-specified Register.

To implement, simply write any data to the register.

(Caution)

When writing to the frame buffer directly after executing this command, write cannot be performed normally. Wait for at least 84mS or longer, or confirm that bit 0 changes from 1 to 0 before shifting to the next write operation. (Bit 0 is the BUSY bit which outputs 1 directly after a hard clear command is issued, and goes back to 0 when completed.) And, during the hard fill operation, avoid executing other drawing functions (Line Drawing Function, Arbitrary Rectangle Fill-in Function, Image Data Transfer Function), too.

The LCD controller features an INTOUT pin. After the completion of hard fill, the active LOW signal is output from this pin, as shown in the following diagram.

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In addition, the LOW width of the signal (INTOUTPW) is about 1 horizontal period (about 26.7 μsec).

By connecting this signal to the IRQ (interrupt) port of the CPU, the completion of hard fill can be detected by interruption.

INTOUT

H
L

INTOUTPW

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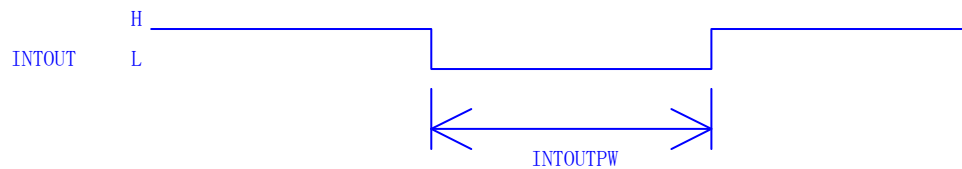
12. External Dimensions

● KS-LTSV-SD (LVDS)

Sign	MIN(mm)	NOM(mm)	MAX(mm)
A			4.10
A1	0.25		0.5
A2	3.2	3.4	3.6
D	30.60 BSC		
E1	28.00 BSC		
e	0.50 BSC		
b	0.17	—	0.27
c	0.09	—	0.20
L	0.45	0.60	0.75
N	208		

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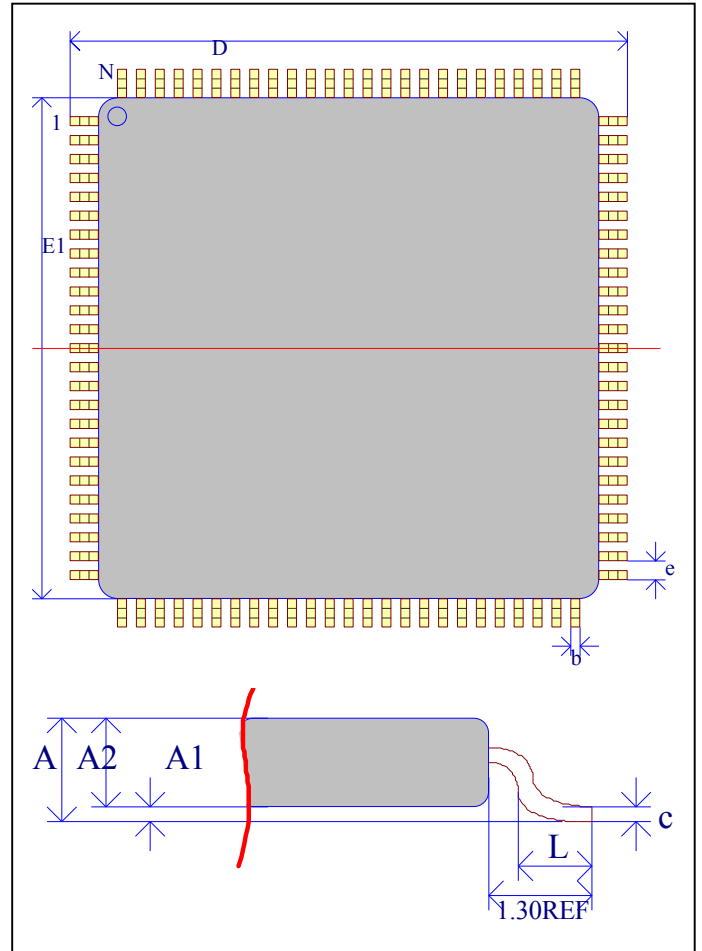
13. Design Precautions

1) When Powering on

The LCD controller is a type that forwards configuration data from the flash memory inside the device to the SRAM.

After powering on, it starts quickly after disengaging the reset. However, the hard fill starts soon after powering on. When designing software, ensure that it checks the completion of the hard fill in the hard fill register before allowing read-write access.

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14. Handling Precautions

1) Transport

Handle the Product and the packaging carefully. Do not throw or drop, as this can cause damage to the Product. When transporting, avoid mechanical vibration and shock as much as possible.

Moreover, avoid the Product getting wet during times of rain and snow, as it has a negative influence on the effectiveness of the antistatic materials (magazine, etc.) and the main Product itself.

2) Storage

① Avoid storing in areas at risk of water leakage and direct sunlight (be particularly careful during times of rain and snow.)

② Do not stack packaging boxes upside down or sideways.

③ The recommended ambient conditions for storage are a constant temperature and humidity in the ranges of 5~35℃ and 40~75%, respectively.

④ Avoid storing in areas prone to noxious fumes (in particular, corrosive gases) and high levels of dust.

⑤ Sudden temperature changes during storage result in condensation, causing the oxidation of leads and corrosion, and thus the deterioration of solder wettability. Store in areas not subject to frequent changes in temperature.

⑥ After taking the Product out of the package, use an antistatic container when storing again.

⑦ When storing, do not directly apply any loads on the Product.

⑧ After an extended period of normal storage (2 years or more), it is recommended to check the solderability and electrical characteristics before use.

3) Inspection

(1) Grounding

① Properly ground the floor, worktable, conveyor, floor mat, etc. so as to avoid a buildup of static electricity. In particular, always ground the worktable which has direct contact with the device and the antistatic floor mat ($100k \sim 100M\Omega/cm^2$).

② Always ground the electronic measuring instruments, the jig, and the soldering iron.

③ Workers should wear antistatic work wear, and the worker's body should be

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grounded using an antistatic wrist strap. The antistatic wrist strap should be grounded at a resistance of about 0.5~1.0MΩ.

(2) Electrical Leakage

Leakage from the electrical inspection equipment and/or the Product-embedded system itself should be avoided to prevent damage to the semiconductors in the device, but above all for the worker's safety. Prior to using the circuit tester, curve tracer, synchroscope, other measuring instruments or other equipment such as the soldering iron that directly comes into contact with the Product, ensure that there is no leakage before grounding.

(3) Order of Inspection

① Before inspecting the Product, check for proper grounding and any leakage as described above. Additionally, apply voltage to the Product only after inserting into a jig. When doing so, avoid sudden startups and shut downs of the power supply.

② After completing inspection of the Product, switch off the applied voltage before removing it from the jig. If removed while powered on, deterioration and/or damage to the Product may occur.

(4) Electric Shock

During electrical measurement, there is possibility of electric shock from the lead or wiring, the connectors, the envelope, and/or the heat sink. Avoid bodily contact while powered on.

4) ESD (Deterioration/Damage from Electrostatic Discharge)

When handling the Product by itself, ensure that the environment is as static-free as possible, workers wear antistatic clothes, containers that have direct contact with the Product use antistatic material, and that proper grounding is used, with a resistance of 0.5~1.0MΩ.

(1) Management of the Work Environment

① When humidity decreases, static electricity can build up through friction. The recommended humidity level is 40~60%, after considering moisture absorption caused by the opening of moisture proof product packaging.

② Ground all equipment and jigs installed within the workspace.

③ Place and ground conductive mats on the workspace floor to prevent static electricity buildup on the floor (surface resistance 10^4~10^8Ω/sq., resistance between surface and grounding 7.5×10^5~10^8Ω/sq.).

④ Place and ground conductive mats (with resistance capability) on the worktable surface to diffuse static electricity (surface resistance:

10^4~10^8Ω/sq. resistance between surface and grounding: $7.5×10^5$~10^8Ω/sq.). Avoid using a metal surface for the worktable that can create a sudden electrostatic discharge with low resistance when the Product comes into direct contact with it.

⑤ When using automated equipment, be careful of the following points.

(a) When picking up the IC package surface by vacuum, use conductive rubber at the pickup's tip to prevent electrostatic buildup.

(b) Minimize friction to the IC package surface. When friction can't be avoided due to the system, decrease the friction surface, or use materials with a smaller friction coefficient or electrical resistance, or consider using an ionizer.

(c) Use electrostatic dissipation materials for parts that come into contact with the lead pin of the Product.

(d) Avoid the Product coming into contact with electrostatically-charged objects (human body, work clothes, etc.).

(e) Utilize a tape carrier that uses a low-resistance material in the part where the tape comes into contact.

(f) Avoid contact between the jig equipment and the Product during the manufacturing process.

(g) For manufacturing processes that cause the package to become electrostatically charged, use an ionizer to neutralize the charge.

⑥ In the workspace, use a VDT filter to prevent electrostatic buildup on the CRT surface, and avoid switching on and off as much as possible during work. This is to prevent electromagnetic induction to the device.

⑦ Regularly measure the electrostatic potential of the workspace, to ensure that there is no buildup.

⑧ Use antistatic fiber covers on chairs, and ground the chairs to the floor with a grounding chain. (Resistance between chair surface and grounding chain: $7.5×10^5$~10^{12}Ω/sq.)

⑨ Place antistatic mats on storage shelf surfaces.
(Surface resistance: 10^4~10^8Ω/sq., resistance between surface and grounding: $7.5×10^5$~10^8Ω/sq.)

⑩ For shipping and temporary storage containers for the device (box, jig, bag, etc.), use a container made of electrostatic dissipation or antistatic material.

⑪ As for carts, use electrostatically conductive materials for surfaces that come into contact with the Product packaging, and ground to the floor by using a

grounding chain. (Resistance between cart surface and grounding chain: $7.5 \times 10^5 \sim 10^{10} \Omega/\text{sq.}$)

⑫ For electrostatically-controlled areas, place a grounding conductor exclusively for static electricity. For this grounding conductor, use a power transmission grounding conductor (class three and above or equivalent) or underground grounding conductor. In addition, it is recommended to separate it from the equipment grounding when feasible.

(2) Work Precautions

① Workers should wear anti-static clothes and conductive shoes (or heel strap, leg strap).

② Workers should also wear a wrist strap, grounded with a resistance of about $1.0 M\Omega$.

③ Ground the tip of the soldering iron, and use with a low voltage (6V~24V).

④ Tweezers have a potential of contacting the Product's pins; as such, use an antistatic type and avoid metal tweezers as much as possible. With low resistance, metal tweezers can cause a sudden discharge from a charged Product. When utilizing vacuum tweezers, use a conductivity adsorption pad on the tip and ground using a grounding conductor exclusively for static electricity. (Resistance: $10^4 \sim 10^{10} \Omega$)

⑤ Do not place the Product and its container near areas with a high electric field (eg. on the CRT, etc.).

⑥ When stacking PCBs with mounted semiconductors, place antistatic boards in between to avoid direct contact. Otherwise, static buildup and discharge may occur.

⑦ When bringing in items into an electrostatically-controlled area (clipboard, etc.), use items made of antistatic material as much as possible.

⑧ When touching the Product directly, wear antistatic gloves or finger cots/stalls. (Resistance: $10^8 \Omega$ and under)

⑨ When placing safety covers for equipment near the device, use covers with a resistance of $10^9 \Omega$ and under.

⑩ When use of a wrist strap is impossible, and friction to the device is likely, use an ionizer.

5) Disposal Precaution

When disposing of the device and the packaging. Please consider the environment and follow all local laws and regulations.

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15. Operating Condition Precautions

1) Ambient Temperature

As a rule, semiconductors are more sensitive to the temperature than other components. As the various electrical characteristics are limited by operating temperature, determine the temperature environment in advance, and consider derating when designing the device. Furthermore, use of the Product beyond specifications not only means that the electrical characteristics cannot be guaranteed, but can also cause deterioration of the device.

2) Ambient Humidity

Molded devices are not perfectly airtight. Therefore, long-term use in highly humid environments can cause deterioration and damage to the semiconductor chips due to moisture penetration.

Moreover, for normal PCBs, highly humid environments can lead to lowered impedance between wirings. Therefore, for systems with high signal source impedance, these substrate leaks and leaks between pins in the Product can cause malfunctions. In such cases, consider humidity-proofing the Product surface. On the other hand, in low humidity, damage due to electrostatic discharge can become a problem, so use within a humidity range of 40~60% when not particularly humidity-proofing.

3) Corrosive Gas

Beware that corrosive gas can affect the device and cause deterioration of electrical characteristics.

An example of this is rubber near the device releases sulfuric gas (or condensation in high humidity), resulting in corrosion to leads, crystallization due to chemical reaction between leads and ensuing leakage.

4) Radiation/Cosmic rays

Generally, devices are not designed to resist radiation and cosmic rays. Therefore, for space applications and in environments with radiation, it is necessary to design specific protection for these factors.

5) Intense Electric Field/Magnetic Field

When the Product is exposed to magnetic fields, abnormal phenomenon (impedance variation and increase of current leaks, etc.) can occur due to polarization of the plastic material and the IC chip internals.

There was also a reported case of malfunction due to the installation of the LSI near the deflection yoke of a television set. In such cases, changing the

installation location and/or deploying an electromagnetic shield maybe necessary. In particular, in an alternating magnetic field, a shield is necessary due to the occurrence of electromotive forces.

6)　Vibration/Impact/Stress

Cannon type devices with a hollow interior and those with a ceramic seal are vulnerable to vibration and shock because internal wire connections are not fixed. However, in actual devices, there have been reports that vibration, shock, or stress to soldered parts and connections leading to the snapping of wires. Therefore, care is necessary in designing equipment with a high vibration rate. It is also known that when stress is applied to the semiconductor chip through the package, a change in internal chip resistance can be caused by the Piezo effect. For analog circuits, be careful of stress to the package, as well. In particular, strong vibration, shock, or stress, can cause cracks in the package or chip.

7)　Ambient Light (ultraviolet rays, sunlight, fluorescent lights, lamps, etc.)

When semiconductor devices are exposed to light, malfunctions can occur due to striking voltage caused by a photoelectric effect. In particular, devices with a view of the internal chip are affected by this, so the design should not allow ambient light to enter. Care must be taken as devices other than photo semiconductors and EP-ROMs can be affected by this.

8)　Dust/Oil

Similar to corrosive gas, chemical reactions may occur in the device due to dust or oil. As such, avoid environments where dust and oil can enter the device, since they can affect the device characteristics. Care must be taken in designing optical devices, since, in addition to the above, optical characteristics can be affected.

9)　Smoke/Fire

Semiconductor devices and modular devices are not fire-resistant, and as such, combustion is possible. In such cases, the device may emit toxic gases.

Therefore, avoid areas with open flames, heated elements, and combustible/flammable objects.

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16. Installation Method

The following are the reflow conditions for the LCD controller and touch panel controller. For more details, please make an inquiry to our sales staff.

　1）　LCD Controller 　 KS-LTSV-SD (LVDS)
　　　The peak temperature and the peak temperature times for reflow are subject to the following conditions.

・　Peak Temperature 　・・・ 　245℃（＋0/-5℃）
・　Peak Temperature Time within 5 ℃（240℃~245℃） 　・・・ 　20~40 seconds

　2）　Touch Panel Controller 　KS-R8TPC
　　　The peak temperature and the peak temperature times for reflow are subject to the following conditions.

・　Peak Temperature 　・・・ 　260℃ 　Max.
・　Peak Temperature Time within 5 ℃（255℃~260℃） 　・・・ 　16 seconds max.

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